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ABSTRACT

Background doping polarity is a key parameter in the design of numerous electrical and optoelectronic devices. It is especially critical for avalanche photodiodes (APDs). Recently, high-performance APDs have been demonstrated based on the AlInAsSb digital alloy materials system. A critical element of this work was the determination of the background doping polarity of the molecular beam epitaxial grown wafers. In this work, we determine the unintentional background doping polarity of $\text{Al}_{0.7}\text{InAsSb}$ using the double mesa capacitance-voltage technique. We fabricated two p-i-n $\text{Al}_{0.7}\text{InAsSb}$ structures: one with p-type background polarity and the other with n-type. The measurements indicate that devices with different background doping polarities show different capacitance relations to the mesa diameters; moreover, the relationship reverses at high voltage in a p-type background device. Subsequent simulations reveal that this reversal is caused by electrical field confinement after the depletion reaches the smaller top mesa. These findings are consistent with reports of reduced surface leakage current in double and triple mesa structures.

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Recently, we have demonstrated high-performance avalanche photodiodes (APDs) based on the $\text{Al}_x\text{In}_{1-x}\text{As}_y\text{Sb}_{1-y}$ (hereafter referred to as AlInAsSb) digital alloy materials system.¹⁻⁴ These devices show high-gain, low-dark current density, extremely low excess noise ($k \sim 0.01$), and high-temperature stability compared to conventional III-V materials. The background doping polarity and concentration are critical parameters for designing complex APDs. For example, in separate absorption, charge, and multiplication (SACM) APDs,^{5,6} the background doping polarity affects the electric field distribution in the absorber and multiplication layers and influences gain and dark currents. Similarly, for staircase APDs,^{7,8} the background doping polarity can modify the electric field distribution, which ultimately determines the probability of impact ionization, and thus the gain, excess noise, and dark current performance of the detector. With respect to using double and triple mesa structures to reduce the surface current in APDs,^{9,10} the background doping polarity is especially important as it determines whether the depletion reaches the smaller mesa, thereby determining how much voltage is required to suppress the electric field at the periphery. This concept will be further studied in this paper.

Background carrier polarity is affected by various uncontrollable factors, many of which arise during the material growth process. Lattice structure, material constituents, and impurity incorporation based on vacuum quality and growth temperature are just a few of the factors that contribute to the defect type and density in a material. Taken together, these form a picture of total background doping that has big impacts on the material. This is often exacerbated for superlattice materials owing to the complex layer structures and interfaces as well as the many constituents that form them.^{11,12} Digital-alloy-based AlInAsSb is a short-period super-lattice structure composed of four binary alloys.¹³ Therefore, it is critical to determine its background doping in order to accurately design complex APDs structures.

Various approaches have been employed to determine the background doping polarity and concentrations, such as Hall measurements,¹⁴ electrochemical capacitance-voltage (ECV) measurements,¹⁵ and secondary ion mass spectrometry (SIMS).¹⁶ Background doping is difficult to determine by Hall measurements on conductive substrates, such as GaSb ¹⁷ due to a native point defect on which the AlInAsSb materials system is grown; ECV measurements are destructive to the

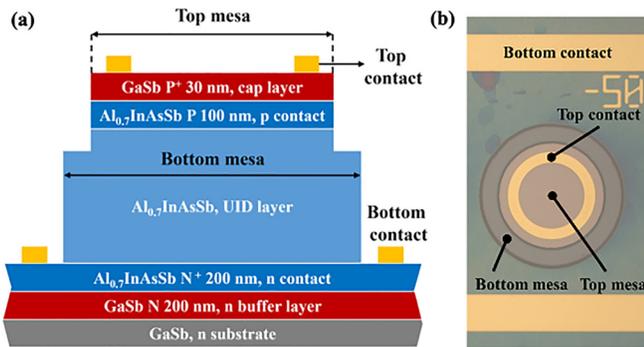


FIG. 1. (a) Schematic cross section of the $\text{Al}_{0.7}\text{InAsSb}$ APDs with an over-etched double mesa structure. (b) Top view of a fabricated device. The doping concentrations are as follows: (1) $\text{GaSb P}^+ 1 \times 10^{19} \text{ cm}^{-3}$; (2) $\text{Al}_{0.7}\text{InAsSb P } 5 \times 10^{18} \text{ cm}^{-3}$; (3) $\text{Al}_{0.7}\text{InAsSb}$, unintentionally doped; (4) $\text{Al}_{0.7}\text{InAsSb N } 5 \times 10^{18} \text{ cm}^{-3}$; (5) $\text{GaSb N } 1 \times 10^{18} \text{ cm}^{-3}$; (6) GaSb substrate. The UID layer thickness is 1000 and 887 nm for sample A and sample B, respectively.

device and limited by low-measurement frequencies; SIMS measurements require extensive calibrations and are often not accurate enough for low-density atoms such background dopants.

Recently, an approach for determining the background polarity was reported by performing the capacitance–voltage (C-V) measurements on over-etched double mesa structures.¹⁸ This approach is based on the dependence of capacitance with the cross-sectional area of a p-n junction. As a result, if fabricated with varying top and bottom mesa sizes, n-type and p-type background doping polarities manifest themselves as different capacitance relations to the diameter of either the top mesa (for n-type) or the bottom mesa (for p-type). This approach has proved superior to conventional approaches as it is straightforward, nondestructive, and independent of substrate type.

In this paper, we investigated the background doping polarity of p-i-n APDs based on $\text{Al}_{0.7}\text{InAsSb}$. The performance of devices with different background doping polarities was compared through C-V and low-temperature measurements. These results lay the foundation for further design of APDs based on the AlInAsSb digital alloy and could be applied to other materials systems as well.

Two homojunction p-i-n $\text{Al}_{0.7}\text{InAsSb}$ samples grown at different times were selected for this study. The layers of these samples were grown by molecular beam epitaxy as a digital alloy of four binary alloys, AlAs , AlSb , InAs , and InSb lattice matched to GaSb substrate.¹³ As shown in Fig. 1, the samples were fabricated into double mesa structures with variations in the bottom and top mesa diameters. Our convention for referring to the double mesa structures is given by $d_{\text{bottom_mesa}}-d_{\text{top_mesa}}$. For example, 200–150 μm represents a double mesa structure with a bottom mesa diameter of 200 μm and top mesa diameter of 150 μm . The mesas were formed by etching in citric acid wet etching that has shown a good isotropic etching to AlInAsSb .¹⁹ SU8 was used for surface passivation. After fabrication, C-V characteristics were measured for many double mesa size combinations. Low-temperature C-V measurements were also performed in a cryogenic chamber from 80 to 350 K. In parallel, modeling tools in Lumerical software were used to simulate the electric field profiles in order to further understand the capacitance characteristics of the double mesa structures.

Different top and bottom mesa diameters were fabricated for this study. Figure 2 shows the C-V curves of sample A with different mesa sizes. The background doping concentration can be estimated by the C-V curve to be around $3 \times 10^{16} \text{ cm}^{-3}$.²⁰ A notable trend is that the C-V curves behave differently at high- and low-bias voltages. At low bias, the capacitance is independent of the top mesa diameter but begins to exhibit separation above -17 V . To further investigate this trend, the capacitance of the devices at -15 and -30 V was extracted and is plotted in Fig. 3 with a comparison to the theoretical capacitance. The red squares in Fig. 3 represent the measured capacitance of the double mesa structure with a mesa diameter shown by the horizontal axis as well as the number inside the figure. The number represents the size of another mesa that is not marked by the horizontal axis. For example, the very left red square in Fig. 3(a) represents the measured capacitance of a double mesa structure that has a top mesa diameter of 80 μm and a bottom mesa diameter of 100 μm . The dashed line is the theoretical capacitance calculated using the following expression:

$$C = \frac{\epsilon\pi\left(\frac{d}{2}\right)^2}{w_d},$$

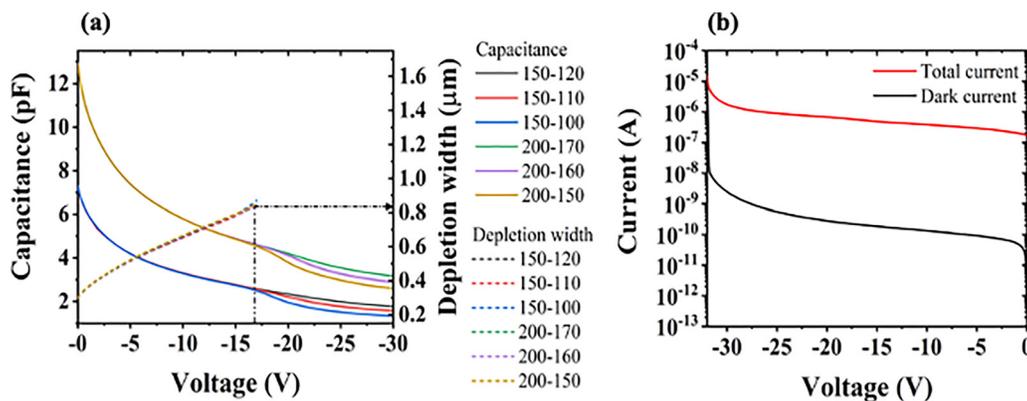


FIG. 2. Measured capacitance-voltage curves of double mesa devices with different top and bottom mesa diameters from sample A. The legend refers to the mesa size of $d_{\text{bottom_mesa}} - d_{\text{top_mesa}} \mu\text{m}$. (b) Current–voltage curves of a 150–100 μm double mesa device on sample A. The total current was measured under flood illumination with a lamp.

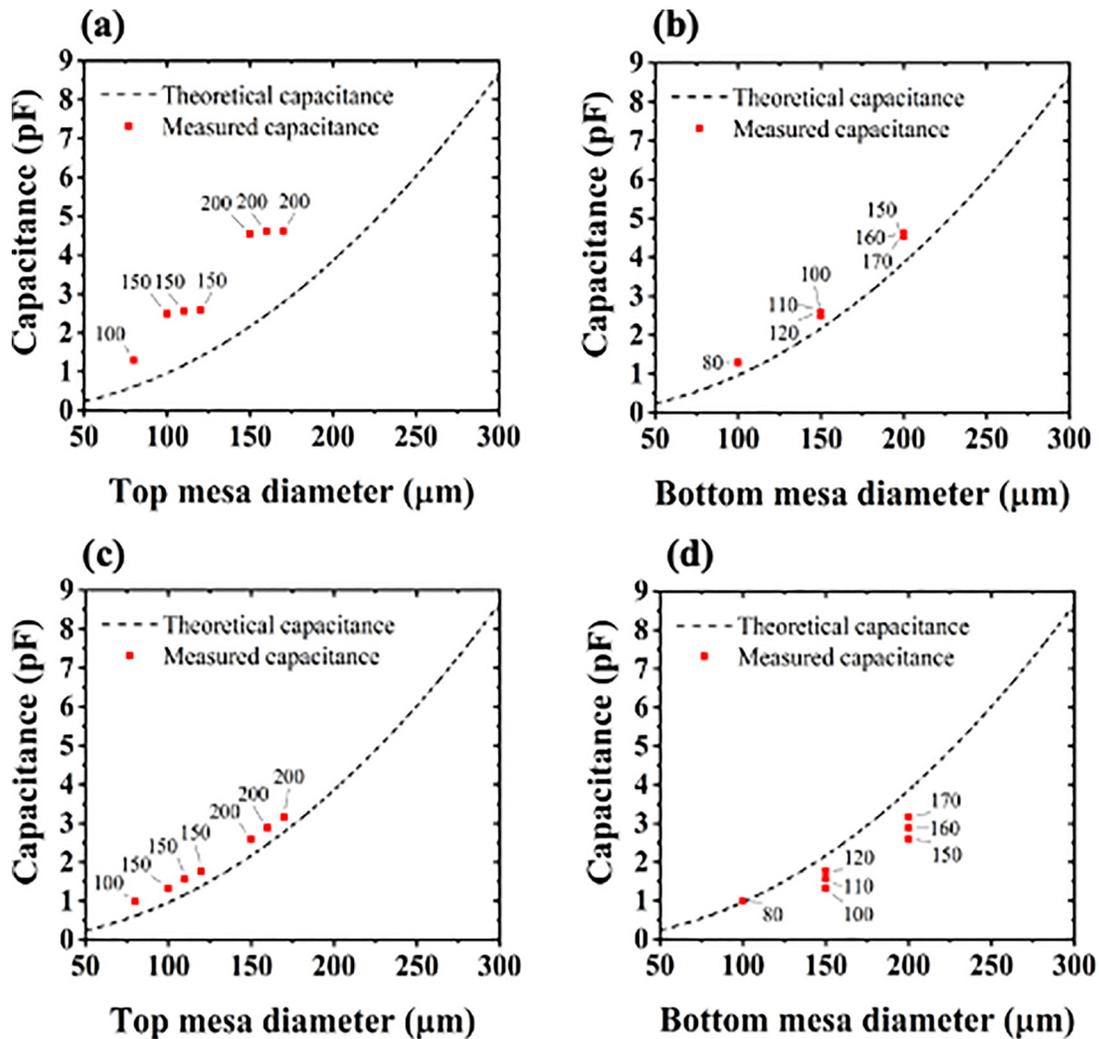


FIG. 3. Measured capacitance of double mesa devices from sample A compared with the theoretical capacitance calculated using either the top mesa diameter or bottom mesa diameter. The capacitance is measured at -15 V in (a) and (b) and measured at -30 V in (c) and (d).

where C is the theoretical capacitance, ϵ is the permittivity, d is the mesa diameter, and w_d is the depletion width. Figures 3(a) and 3(b) show that below -17 V, the capacitance is a function of the bottom mesa diameter but independent of the top mesa diameter. The measured capacitance fits well with the theoretical capacitance calculated using the bottom mesa diameter, except that the measured capacitance is slightly higher. The reason for this is that as indicated in Fig. 2, the device is not yet fully depleted at -15 V. This trend indicates a p-type background doping in the UID layer, which causes the depletion to begin from the p-n junction between the p-type UID layer and the N contact layer. As a result, the capacitance is determined by the area of the bottom mesa. However, this trend reverses at high bias. Beyond -17 V, the C-V curves of devices with different top mesa diameters begin to separate. It is worth noting that with the same bottom mesa diameter, devices that have smaller top mesas begin to show lower capacitance. As shown in Figs. 3(c) and 3(d), the capacitance is better

determined by the top mesa diameter at -30 V and fits well with the theoretical capacitance calculated using these sizes. This is exactly opposite to the trend prior to -17 V.

The number inside the figure represents the size of another mesa that is not marked by the horizontal axis.

To further understand the reversal of the capacitance behavior with respect to mesa area, the electric field profile within the device was simulated with the Lumerical CHARGE solver,²¹ as shown in Fig. 4. At low reverse bias in Fig. 4(a), high electric field develops around the p-n junction formed by the p-type UID layer and bottom N contact layer. This behavior matches Figs. 3(a) and 3(b), where the measured capacitance is determined by the bottom mesa, as the effective junction area is equal to the area of the bottom mesa. Then, as the reverse bias is increased further, the depletion reaches the narrower top mesa, and the electric field becomes confined beneath the top mesa. As a result, the capacitance begins to decrease with the

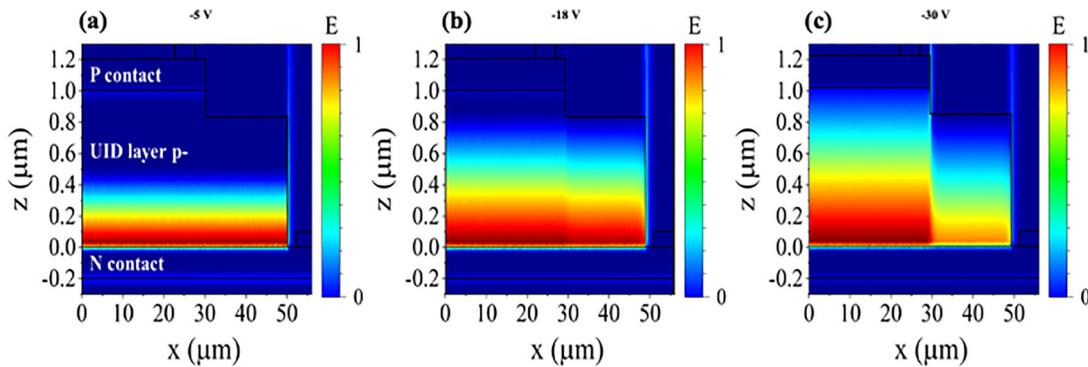


FIG. 4. Normalized distribution of the electric field magnitude E inside the double mesa devices from sample A (p-type background).

decreasing effective area. This simulation closely follows the trend shown in Fig. 2. It follows that in order to determine the background polarity, it is better to analyze the capacitance at low bias when the effect of only one mesa dominates. Moreover, the depletion width at -17 V where the capacitance curves begin to separate is approximately 840 nm, which matches the measured between the bottom of the p-type UID layer and the top of the bottom mesa after etching, which further supports the finding of the simulation that the condition that causes the capacitance to decrease is the depletion width reaching the smaller top mesa. It is also worth noting that the capacitance at -30 V is slightly higher than the theoretical capacitance. This could be due to the high background carrier concentration of the device, which prevents the device from fully depleting before it breaks down between -30 and -31 V. On the other hand, the lateral field extension may also have an influence. As shown in Fig. 4(c), there is still a portion of the electric field that extends beyond the confines of the top mesa region even at high reverse bias. As a result, the effective junction area may be slightly larger than the top mesa area alone.

The decrease in the electric field at the periphery of the bottom mesa illustrated in Fig. 4 has been used to successfully reduce the surface leakage dark current in APDs with multiple mesas.^{9,10} Different

from ion-implanted doping-based guard ring techniques for CMOS-APDs,^{22,23} this approach is based on mesa structure engineering and suitable for mesa-based APDs. Our analysis further shows that the basic condition for achieving low-surface field and corresponding low-surface leakage is that the depletion must extend to the smaller top mesa. Additional applied bias further extends the depletion region into the smaller mesa, leading to even stronger the electric field confinement and the lower the surface field will be. This is clearly shown by comparing Figs. 4(b) and 4(c). These results suggest that for a thick or highly doped p-type background depletion layer, a P-down (n-i-p-substrate) structure with the smaller mesa etched on the top N contact would be needed to reduce the surface field, in which case, the depletion can reach the smaller top mesa from the beginning, with a result that the electric field is constantly confined under the top mesa, and the surface field is low. Otherwise, large applied bias may be required before the depletion can reach the top mesa, limiting its effectiveness in reducing the surface field. This high voltage may cause the device to break down before the low dark current can take effect. Similarly, for a thick or highly doped n-type background depletion layer, an N-down (p-i-n-substrate) structure with the smaller mesa etched on the top P contact would be needed in order to reduce the surface field.

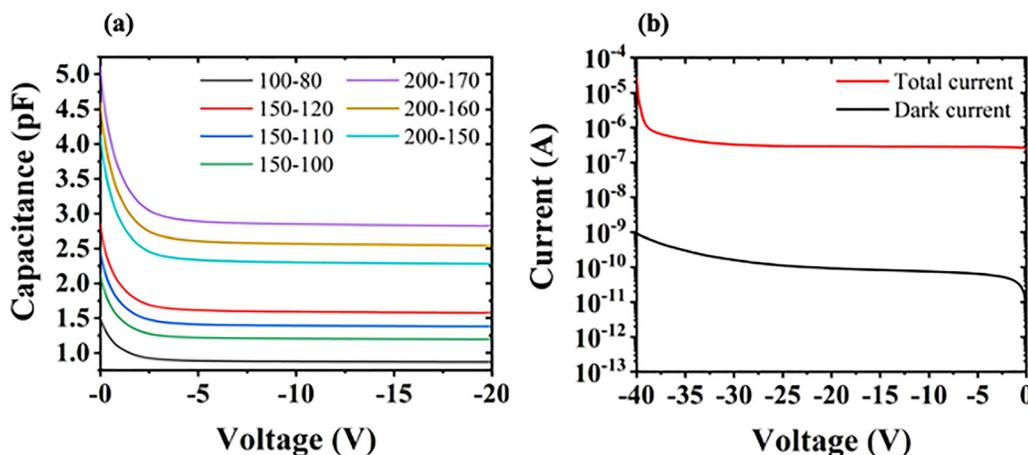


FIG. 5. Measured capacitance-voltage curves of double mesa devices with different top and bottom mesa diameters from sample B. The legend refers to the mesa size of $d_{\text{bottom_mesa}} - d_{\text{top_mesa}}$ μm . (b) Current-voltage curve of a $150-100$ μm double mesa device on sample A. The total current was measured under flood illumination with a lamp.

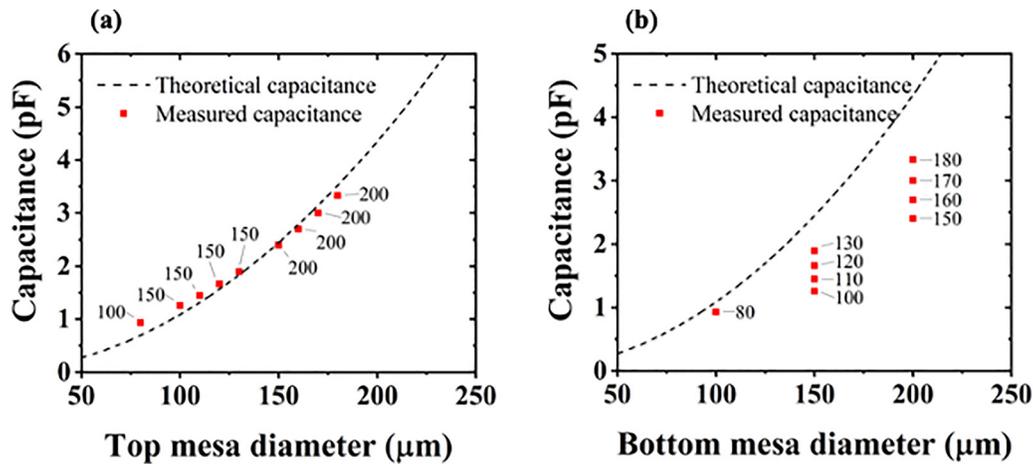


FIG. 6. Measured capacitance of double mesa devices from sample B compared to the theoretical capacitance calculated using either (a) top mesa diameter or (b) bottom mesa diameter. The capacitance is measured at -30 V. The number inside the figure represents the size of another mesa that is not marked by the horizontal axis.

Figure 5 shows the C-V curves of the devices from sample B with different mesa sizes. The background doping concentration can be estimated by the C-V curve to be around $6 \times 10^{15} \text{ cm}^{-3}$.²⁰ The C-V behavior of sample B is distinctly different from that of sample A. The measured capacitance of sample B varies with different top mesa sizes, unlike the bottom mesa dependence demonstrated by sample A. Similar to our analysis for sample A, the measured capacitance of sample B at -20 V is plotted with the theoretical capacitance in Fig. 6. It is evident that the capacitance has a clear dependence on the top mesa size and is independent of the bottom mesa diameter. This is a characteristic of an n-type background device, where the depletion starts from the p-n junction between the n-type UID region and the P contact layer in the top mesa. The other difference is that the C-V curves of sample B do not separate at high bias, i.e., they behave like a single mesa p-i-n device. To investigate the mechanism for this difference, the electric field was simulated for the sample B devices shown in Fig. 7. The p-n junction forms at the interface between the top of the n-type UID layer and the bottom of the P contact layer within top mesa. As a result, the depletion initially forms in the top mesa, which determines the effective capacitor area. Contrary to the p-type background devices, the electric field inside the n-type background devices remains confined under the smaller top mesa even when the depletion

extends into the bottom mesa. Therefore, the effective area does not change with the applied bias, and no C-V curve separation is observed.

The low-temperature capacitance of sample B was investigated, since previous research has shown that the background doping in InAs/GaSb superlattices can invert from n-type to p-type when the temperature is reduced.^{24,25} Such polarity change is attributed to the difference in activation energies of p-type and n-type dopant atoms.²⁵ If present, this behavior persists in AlInAsSb; electrical characteristics for AlInAsSb APDs would strongly depend on the operating temperature. Figure 8 shows the measured capacitance of sample B at -20 V and at 80 K. It suggests that the capacitance is still determined by the top mesa diameter, like in Fig. 6. This indicates that a background polarity flip has not occurred in $\text{Al}_{0.7}\text{InAsSb}$ even at cryogenic temperatures. Temperature-independent background polarity can be an important feature for low-temperature operation of AlInAsSb APDs, especially those that are sensitive to high dark currents and may require cooling. The capacitance at 180 and 350 K was also investigated for sample B, which demonstrates the same trend, i.e., the devices consistently show an n-type background behavior. The capacitance does vary with temperature as shown by the $100\text{--}150 \mu\text{m}$ device in Fig. 8(b). This can be attributed to the temperature dependence of the AlInAsSb permittivity.²⁶

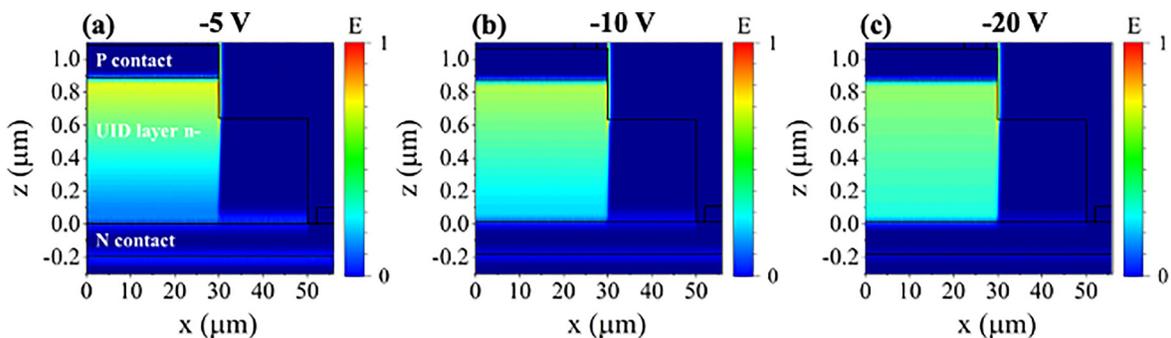


FIG. 7. Normalized distribution of the electric field magnitude E inside the double mesa devices on sample B (n-type background).

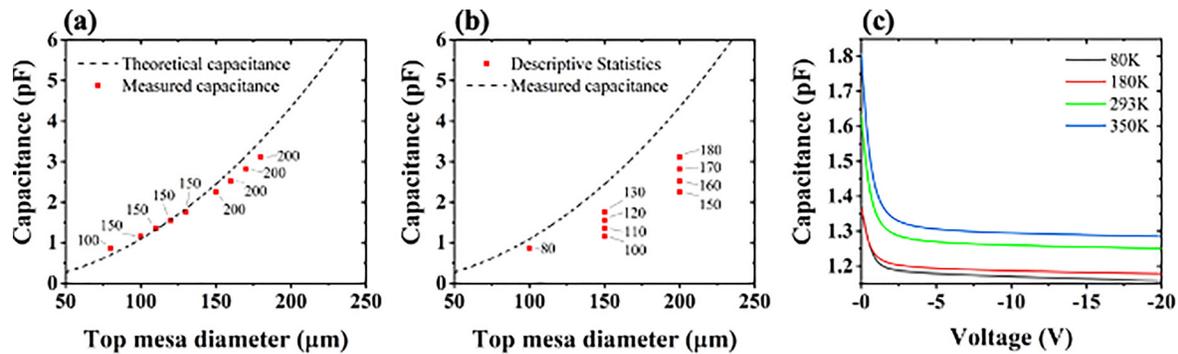


FIG. 8. Measured capacitance at 80 K of double mesa devices from sample B compared to the theoretical capacitance calculated using either (a) top mesa diameter or (b) bottom mesa diameter. The number inside the figure represents the size of another mesa that is not marked by the horizontal axis. (c) Capacitance–voltage curves of the 150–100 μm devices from sample B measured at different temperatures.

We have compared the C-V characteristics of double mesa $\text{Al}_{0.7}\text{InAsSb}$ p-i-ns with different background doping polarities. The C-V measurements reveal that the background carrier polarity at low-bias is determined by the top mesa diameter for devices with an n-type background polarity and by the bottom mesa diameter for a p-type background polarity. Identifying the background doping polarity is critical for the AlInAsSb APD design, especially for staircase and SACM APDs, where the polarity-dependent band bending plays an important role in the device operation. It was also found that the areal dependence of the capacitance for the p-type background double mesa structure reverses at high bias, but not for n-type background structures. This was found to result from the electric field confinement in the smaller top mesa region. The enhanced field confinement presented here can guide the design of double or triple mesa structures to suppress surface leakage dark current, i.e., a P-down structure is preferred for a p-type background device, and an N-down structure is preferred for a n-type background device.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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