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Cite as: J. Appl. Phys. **126**, 043101 (2019); <https://doi.org/10.1063/1.5108905>

Submitted: 03 May 2019 . Accepted: 28 June 2019 . Published Online: 22 July 2019

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ABSTRACT

We demonstrate electrical modulation of plasmonic interfaces in semiconductor p-n⁺⁺ junctions fabricated from both III-V and Si materials. Junction diodes are grown/fabricated, consisting of degenerately doped n-type material and heavily doped p-type material, where the n⁺⁺ semiconductor acts as a plasmonic material capable of supporting infrared propagating surface plasmon polaritons. Devices were characterized electrically and optically, and we achieved tuning of the reflectivity under applied bias with amplitude reaching 1.5% in mid-IR wavelengths. We developed a model of electrical carrier injection at the degenerately doped interface, which we used to model the bias-dependent optical properties of the system. A strong agreement between our model and experimental results is demonstrated. The presented devices offer the opportunity for electrical modulation of propagating plasmonic modes in an all-semiconductor system.

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I. INTRODUCTION

The field of plasmonics has been of particular interest for next generation photonic structures and devices due to the potential for subwavelength confinement of optical modes, offering new approaches for subwavelength imaging,^{1–3} sensing,^{4–7} and waveguiding.^{8,9} At short wavelengths (visible to near-IR), the plasmonic materials of choice are the noble metals (i.e., Ag, Au), which offer the negative permittivity (ϵ_m greater in magnitude, opposite in sign to the surrounding dielectric material permittivity ϵ_d) required to sustain surface plasmon polaritons (SPPs),¹⁰ with reasonably low losses. But at longer wavelengths, such as the mid-infrared (mid-IR, $\lambda \sim 2–20 \mu\text{m}$), the optical behavior of noble metals more closely resembles that of perfect electrical conductors ($\epsilon_m \rightarrow -\infty$) than that of plasmonic materials, precluding the subwavelength mode volumes that have long been a primary motivation for plasmonic structures.^{11,12} However, alternative materials, having lower free-carrier concentrations, can serve as long-wavelength plasmonic materials for IR applications.^{13,14} One such material is graphene, whose monolayer thickness, unique band structure, and electrically controllable optical properties have driven significant interest in tunable graphene plasmonic devices for the mid-IR and terahertz (THz) spectral range.¹⁵ Modulation of free-space THz light using gate-tunable 2D graphene metamaterials has been demonstrated,¹⁶ and architectures have been proposed for modulation of mid-IR

surface plasmon polaritons on graphene.¹⁷ Though graphene boasts a number of unique properties for the development of mid-IR plasmonic structures and devices, the development of defect-free, large-area graphene remains challenging, and typical graphene plasmonic architectures require the heterogeneous integration of multiple materials systems.

Alternatively, opportunities exist to develop all-semiconductor active plasmonic devices grown monolithically by epitaxial techniques. Such an approach would take advantage of degenerately doped semiconductors that offer plasma frequencies [ω_p , where $\epsilon_m(\omega_p) \approx 0$] across the mid-IR by control of dopant, and thus free carrier, concentrations. The high carrier concentrations required for plasmonic behavior in the mid-IR can be achieved in Si by top-down ion implantation¹⁸ or spin-doping,^{19,20} or in III-V materials during (bottom-up) epitaxial growth.^{21–24} Both the top-down and bottom-up approaches allow for the development of semiconductor device architectures with integrated plasmonic materials. The former allows for direct integration of mid-IR plasmonic systems with Si electronics, while the latter offers the potential for layered growth of “metallic” and dielectric materials²⁵ and thus monolithic integration of mid-IR plasmonic structures with mid-IR optoelectronic active regions.²⁶ Both approaches offer the opportunity for the development of a new generation of dynamic plasmonic devices. One such example is the proposed surface plasmon

polariton diode (SPPD),^{27,28} an optoelectronic switch where the propagation of surface plasmon polariton (SPP) bound to a p-n⁺⁺ junction is modulated by charge injection during forward biasing of the junction. Simulated performance of the SPPD suggests potential modulation of up to 98% and switching rates of 100 GHz, which when combined with the SPPD's compatibility with current semiconductor growth/fabrication techniques offers an avenue toward high speed electrical switching of optical signals with sub-wavelength mode volumes.

Here, we present an important step toward the realization of an all-semiconductor active plasmonic device such as the SPPD. Specifically, we performed modulated reflection experiments on p-n⁺⁺ junctions from which we extracted the optical property changes at the junction interfaces induced by minority carrier injection and demonstrate electrical control of the mid-IR optical properties of the p-n⁺⁺ junctions by applied bias. We investigated p-n⁺⁺ junctions grown epitaxially on InP and fabricated by spin-doping on Si-on-insulator (SOI) wafers. We characterized our devices both electrically and optically and measured the change in the optical properties as a function of forward bias. We modeled the band structure and carrier concentration as a function of position for both devices and employed this model to inform simulations of the device's optical properties as a function of applied bias. Our simulations closely matched our experimental data and indicate the potential of the presented device architectures for integration into SPPD devices. In this work, we investigate the modulated reflection of quasi-plane waves from the p-n⁺⁺ interface, not the modulation of SPP modes in the SPPD configuration.^{24,25} Though our fractional modulation of reflectivity is significantly smaller than the fractional modulation predicted for SPPs in the SPPD configuration, from our experimental data, we are able to extract the dynamic optical properties of our plasmonic interface and determine their suitability for the SPPD architecture.

II. DEVICE GROWTH, FABRICATION, AND EXPERIMENTAL SETUP

The InGaAs device was grown by molecular beam epitaxy on a Varian Gen-II solid-source molecular beam epitaxy (MBE) system with a valved arsenic cracker and effusion sources for gallium and indium. Effusion cells were also used for the dopants, silicon (n) and beryllium (p). The InGaAs diode was grown lattice-matched to a (100) InP substrate and consists of 1 μm of n⁺⁺-In_{0.53}Ga_{0.47}As ($n = 3.4 \times 10^{19} \text{ cm}^{-3}$) followed by 750 nm of p-In_{0.53}Ga_{0.47}As ($p = 1 \times 10^{18} \text{ cm}^{-3}$). A low growth rate was used ($\sim 0.5 \mu\text{m/h}$) in order to obtain the high dopant concentration for the n⁺⁺-InGaAs. The Si device is fabricated from an SOI wafer with 1 μm SiO₂ and a 2 μm p-doped ($N_A = 1 \times 10^{18} \text{ cm}^{-3}$) Si active region. First, the wafer was spin-coated with a 15% phosphorus concentration spin-on glass dopant (Filmtronics, P509), prebaked (400 °C, 105 s), and then annealed (950 °C, 40 min) in an N₂ environment, driving the phosphorus dopants into the Si active layer. Following the anneal, the dopant film was removed with a buffered oxide etch and the now-doped SOI wafer was diced, along with a Si handle wafer, into square pieces of the same size. Ti/Au (5/125 nm) was evaporated on both the SOI and the handle wafer, and then the two metal-coated samples were Au/Au bonded at 9 MPa pressure and 400 °C for

20 min. The SOI wafer substrate was then removed using a deep silicon etcher, followed by a buffered oxide etch to remove the SiO₂ layer. Infrared reflectivity measurements were performed on the Si sample after each fabrication step, which were later used to extract the doping profile of the final device. Both Si and InGaAs samples were then fabricated into mesa devices, with the mesas ($390 \times 290 \mu\text{m}^2$) formed by standard UV photolithography and then dry etched in an Oxford ICP etcher. The SOI sample was etched using HBr/Cl₂ (45/5 sccm, 1450 nm etch depth) and the InGaAs sample was etched using Cl₂/CH₄/H₂ (6/4/7 sccm, 1080 nm etch depth). Top and bottom contacts were then defined by photolithography, metallization (Ti/Au, 5/125 nm), and lift-off. The top contacts are designed with a large bond pad ($100 \times 200 \mu\text{m}^2$) and four window panes separated by 20 μm contact stripes. Schematics of the initial wafers and final device structures are shown in Figs. 1(a) and 1(b). The samples were then mounted to copper mounting blocks and wire-bonded to stand-off ceramic pads.

All samples were characterized by reflection spectroscopy using a Bruker v80V Fourier transform infrared (FTIR) spectrometer and a mid-IR microscope operating in rapid-scan mode and normalized to reflection from a gold surface (which in the mid-IR has $\sim 100\%$ reflectivity). Upon fabrication, we measured the

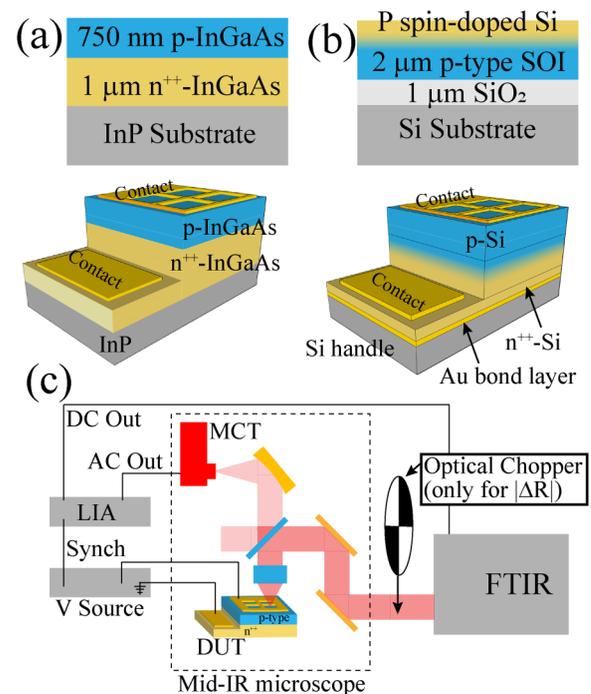


FIG. 1. (a) Epitaxial layer structure and device layout for the InGaAs p-n⁺⁺ diode grown on InP. (b) Layer structure for the P spin-doped SOI wafer, and device schematic for the spin-doped p-n⁺⁺ diode following wafer bonding, substrate removal, and device fabrication. (c) Experimental setup for amplitude modulation step-scan measurement of reflection modulation ($|\Delta R|$) from the biased devices. The optical chopper pictured in (c) is used only for the measurement of $I_R(\lambda, 0)$ in order to calculate $|\Delta R(\lambda)|$.

current-voltage (IV) characteristics of each device. Finally, we measured the change in reflectivity under applied bias using the experimental setup shown in Fig. 1(c), where source light from the FTIR is directed to the sample surface by, and the reflected light collected through, the mid-IR microscope's internal beam splitter and objective lens. The reflected light is apertured in the image plane so that we only collect light reflected from an area enclosing the four window panes of our top contact. The p-n⁺⁺ junction diode was then driven by a 10 kHz square wave voltage signal and the reflected signal measured by the microscope's HgCdTe (MCT) detector, whose output was fed into a lock-in amplifier (LIA), referenced to the voltage source. We use a 10 kHz modulation frequency in order to minimize any photothermal effects caused by the relatively small power dissipation in the diode (~0.1 W). The FTIR was then operated in the amplitude modulation step-scan mode, and the DC output of the LIA was fed into the FTIR at each mirror position, giving the difference spectrum $|I_R(\lambda, V_a) - I_R(\lambda, 0)|$. In order to determine the change in reflectivity (normalizing for the FTIR source spectrum, optics, and MCT response), an additional spectrum was taken, where the incident light was mechanically chopped before being reflected from the unbiased sample (here the LIA is referenced to the chopper frequency), giving $I_R(\lambda, 0)$. The modulation amplitude of reflectivity was then calculated using $|\Delta R(\lambda)| = |I_R(\lambda, V_a) - I_R(\lambda, 0)|/I_R(\lambda, 0)$. Because our sampling area includes some fraction of the Ti/Au top contact, we included a geometric correction factor to extract the percentage change in reflectivity of the semiconductor device. All measurements were performed at room temperature.

III. EXPERIMENTAL AND NUMERICAL RESULTS

Figure 2 shows the unbiased reflectivity spectra from the samples studied in this work. In Fig. 2(a), the reflectivity from the unbiased, as-grown, InGaAs sample is shown, with all the hallmarks of a finite-thickness Drude metal grown on a high index substrate: 30%–40% reflectivity at short wavelengths (with Fabry-Perot oscillations resulting from thin film interference effects), and a sharp transition to high reflectivity occurring at the n⁺⁺ InGaAs plasma wavelength. The experimental data were compared with the theory. A numerical framework was developed to self-consistently study the relevant electrical, thermal, and optical properties of the junction. To account for the above multiphysics contributions, we implemented the finite difference integrated COMSOL software by self-consistently coupling the Semiconductor Module (CSM), the Electromagnetic Module (CEM), and the Heat Transfer Module (CHTM). For the InGaAs device, we assumed a doping profile corresponding to an abrupt junction, which is consistent with the atomic precision in layer thickness associated with MBE growth. The CSM and CHTM modules were used to obtain the local electron $n(\vec{r}, T)$ and hole $p(\vec{r}, T)$ densities that are dependent on the local temperature T . The reflectivity was then calculated by modeling the p-n⁺⁺ InGaAs junction as an inhomogeneous Drude metal with contributions from bound and conduction electrons and holes: $\epsilon(\omega, \vec{r}) = \epsilon_b - \frac{\omega_{pn}^2}{\omega(\omega + i\omega_n)} - \frac{\omega_{pp}^2}{\omega(\omega + i\omega_p)}$, where the position and local temperature dependent electron and hole plasma frequencies are given as $\omega_{pn}(\vec{r}, T) = \sqrt{q^2 n(\vec{r}, T)/\epsilon_0 m_e}$

and $\omega_{pp}(\vec{r}, T) = \sqrt{q^2 p(\vec{r}, T)/\epsilon_0 m_h}$, while the bound electron contribution is fixed $\epsilon_b = \epsilon'_b + i\epsilon''_b = 11.64 + i0.01$. The relaxation frequencies in the model are $\omega_n = q/\mu_n m_e$ and $\omega_p = q/\mu_p m_h$ and depend on both the electron and hole mobilities and effective masses, whose values vary with the doping and the local temperatures.²⁹ Excellent correspondence between the experiment and the model is observed, as can be seen in Fig. 2(a).

Figure 2(b) shows the reflectivity of the Si sample following bonding to the Si handle wafer and substrate and oxide removal. A significant spectral structure is seen in the reflectivity for the flip-bonded and substrate-removed Si sample, a result of the finite thickness, and spatially dependent doping concentration, of the n⁺⁺ region, coupled with the high reflectivity of the Au bonding layer. The final silicon device shown in Fig. 2(b) is more difficult to extract optical parameters from, given the continuous variation in doping concentration (and thus plasma wavelength and scattering rate) associated with the diffusion process. To do so, we leveraged the reflection spectra from each step of the Si device fabrication

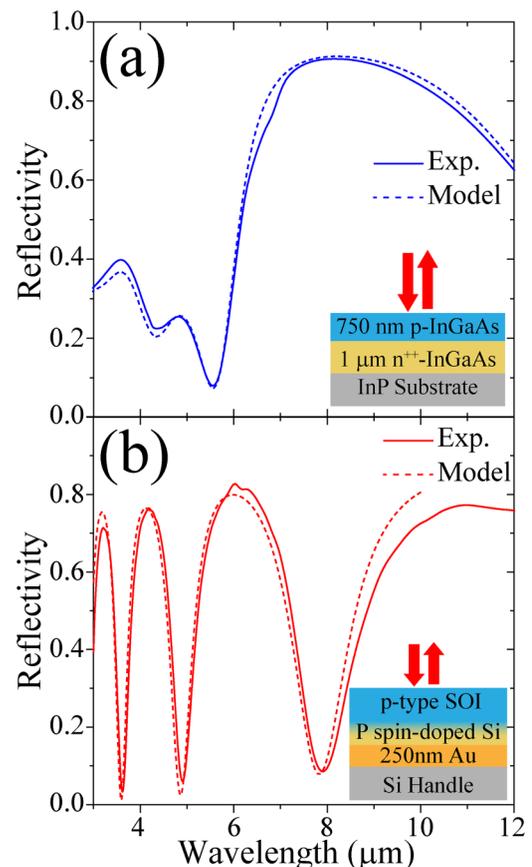


FIG. 2. Reflectivity spectra from (a) as-grown InGaAs p-n⁺⁺ diode and (b) wafer bonded and substrate-removed phosphorus spin-doped, annealed SOI active layer. Solid lines show experimental and dashed lines show finite-element-modeled reflectivity spectra.

process and assumed an *erfc* doping profile for the implanted P-dopants.³⁰ A position-dependent dielectric function was then acquired using a similar method to the InGaAs case with different parameters for Si ($\epsilon_b = 11 + i0.25$) and doping concentration-dependent effective mass accordingly.³¹ The reflectivity spectrum of the Si device was then calculated using the thermo-electro-optic model resulting in an excellent match with experimental data [Fig. 2(b)]. The parameters extracted from the models for both the SOI and InGaAs devices show that the n^{++} layers of each are doped to the point where they are able to support long wave infrared (LWIR, $\sim 8\text{--}12\ \mu\text{m}$) surface plasmon modes at the n^{++} p interfaces.^{32–34} The plasma wavelength of n^{++} InGaAs was determined to be $\lambda_p = 6.85\ \mu\text{m}$, while the most highly doped portion of the n^{++} Si was determined to have $\lambda_p \approx 3.29\ \mu\text{m}$.

Experimental evidence for p- n^{++} junction formation is seen in the IV measurements of both the Si sample and InGaAs sample, shown in Fig. 3(a). Both devices showed the expected forward-biased turn-on associated with diodelike electrical behavior, while the InGaAs device showed a low reverse-bias current turn-on

associated with Zener tunneling in the smaller bandgap InGaAs device.^{35,36} The above-described self-consistent thermo-electro-optic model was used to calculate band structures and carrier concentrations under different applied biases. Figures 3(b) and 3(c) show the modeled band structure for forward biases $V = 0, 0.4, 0.6, 0.95,$ and $1.5\ \text{V}$ for the InGaAs and Si devices, while Figs. 3(d) and 3(e) show the electron and hole concentrations as a function of position for the same applied voltages of the InGaAs and Si devices. Figures 3(b)–3(e) are all expanded around the metallurgical junction to capture the small volumes over which the change in carrier concentration occurs. As would be expected for a forward-biased junction, a significant increase in the minority carrier concentration is observed under applied bias. We modeled the electron concentration on the p-side of the junction increasing from the $\sim 10^5$ to $10^{15}\ \text{cm}^{-3}$ range for the InGaAs device and from the $\sim 10^2$ to $10^{16}\ \text{cm}^{-3}$ range for the Si device. In extreme proximity ($<10\ \text{nm}$) to the junction, injected carrier concentration approaches the equilibrium concentration of the n^{++} material, essentially extending the “plasmonic” interface by a few nanometers. The total changes in charge distribution

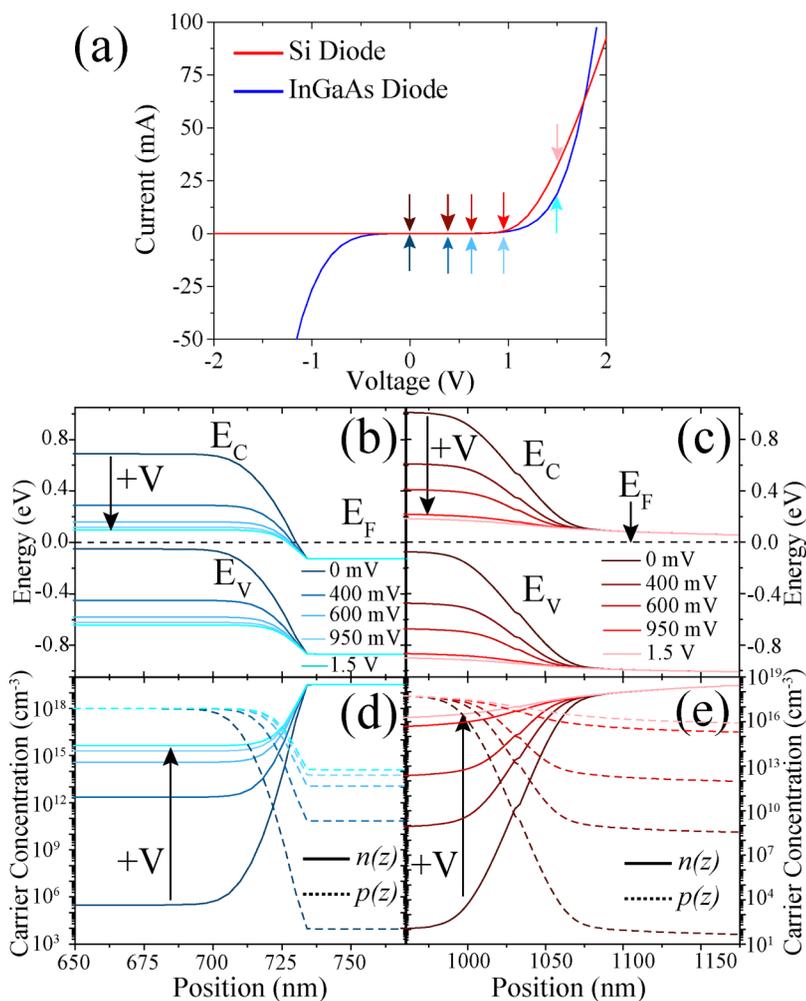


FIG. 3. (a) Experimental current vs voltage curves for InGaAs (blue) and Si (red) p- n^{++} diode devices. Modeled conduction and valence band structures for (b) InGaAs and (c) Si p- n^{++} diode devices, with the zero bias Fermi levels shown as black dashed lines. Modeled free electron (solid) and hole (dashed) concentrations for biased (d) InGaAs and (e) Si biased p- n^{++} diode devices.

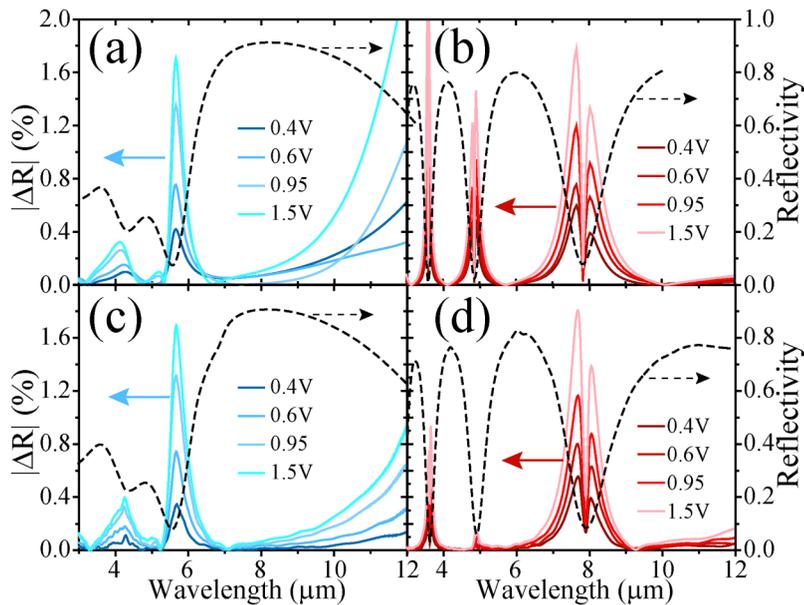


FIG. 4. Modeled percentage change in reflectivity for the (a) InGaAs and (b) Si $p-n^{++}$ junction under forward biases. Experimental percentage change in reflectivity for the (c) InGaAs and (d) Si $p-n^{++}$ junction under forward biases. Zero bias reflectivity (black dashed, right axes) is shown for each sample for comparison.

near the junction, where carrier concentrations approach n^{++} levels over a region of only ~ 10 nm, are rather small (given the total amount of free carriers in the system). However, our model takes into account the voltage spreading due to the window contacts used in this work, which limits the regions of high injection to areas underneath the contacts (which are not optically accessible). The optically accessible portions of the device are limited in the voltage dropped over the junction and thus subsequently limited in the modulation of the optical properties of the structure. Nonetheless, for devices with solid contacts, such as the SPPD, significant and uniform modulation of the plasmonic interface, for control of SPP at the interface, should be achievable.

The modeled carrier concentration, under applied bias, was used to predict the reflectivity of the system as a function of the voltage across the junction using the above-described self-consistent thermo-electro-optic model, taking into account voltage spreading in the window contacts. Figures 4(a) and 4(b) show the modeled change in reflectivity $|\Delta R(\lambda)| = |R(\lambda, V_a) - R(\lambda, 0)|/R(\lambda, 0)$ (equivalent to $|I_R(\lambda, V_a) - I_R(\lambda, 0)|/I_R(\lambda, 0)$ since both the numerator and the denominator are normalized to gold reflection) at each of the applied biases for the InGaAs and Si devices, respectively. By measuring the relative change in reflection, we allow for a clearer picture of the voltage dependence of our devices' optical properties, as the absolute change in reflectivity is small. As can be seen from our models, distinct spectral features associated with the charge injection of the biased junction are observed, with changes in the reflectivity of $>1.5\%$ occurring at the edges of the sharper reflectivity spectral features. Figures 4(c) and 4(d) show the experimental change in reflectivity from the InGaAs and Si samples, respectively, under the same forward biases, with both matching the modeled results well. The exception to the excellent fit is the $\lambda \sim 5\mu\text{m}$ spectral feature observed in the modeled Si sample reflectivity modulation [Fig. 4(b)]. The significantly stronger nature of this feature,

when compared to the experimental data, is believed to result from the slight discrepancy between the unbiased experimental and modeled reflectivity. As can be seen in Fig. 2(b), the reflectivity dip at $\lambda \sim 5\mu\text{m}$ is slightly deeper for the finite element model. Because the unbiased reflectivity appears in the denominator of the $|\Delta R(\lambda)|$ expression, this discrepancy results in an inflated $|\Delta R(\lambda)|$ when compared to the experimental data. For the InGaAs device, we also see some discrepancy between the model and experiment at longer wavelengths, which may be due to stronger frequency dependence of the lattice contribution to the dielectric constant. While the spectral region beyond $10\mu\text{m}$ is of no substantial importance for the current work, this effect can be considered in future studies.

IV. DISCUSSION AND CONCLUSIONS

The overall good agreement between our experimental data and our multiphysics finite element model provides strong experimental support for dynamic modulation of mid-IR plasmonic devices. Our self-consistent thermo-electro-optic simulations indicate that our modulation is the result of minority carrier injection, and not any thermal effects, as the modeled temperature change for the devices investigated is less than 5 K at the highest biases applied (<0.3 K for the Si device, <3 K for the InGaAs device). These results indicate the potential for high speed dynamic modulation of mid-IR plasmonic devices such as the SPPD. While limited tunability was observed from our planar window-contact devices, significantly stronger injection can be achieved with continuous top contacts, such as those used in the SPPD. For such devices, looking to modulate propagating modes at the $p-n^{++}$ interface, open window contacts are not required, and significantly stronger modulation can be achieved.

In conclusion, we have fabricated and characterized both InGaAs and Si $p-n^{++}$ diodes capable of supporting mid-IR surface

plasmon polariton modes at the junction interface. We are able to demonstrate the modulation of the devices' optical properties resulting from minority carrier injection at the junction. Our finite element model for simulating the optical and electrical properties of the fabricated devices matches well with our experimental results, offering insight into the potential achievable improvement in the modulation amplitude for propagating surface modes in these materials. The presented results indicate the potential feasibility of dynamic mid-IR optoelectronic devices leveraging electrical control of plasmonic interfaces supporting infrared surface plasmon polariton modes.

ACKNOWLEDGMENTS

Z.D. and D.W. gratefully acknowledge funding from the National Science Foundation (NSF) (Award No. ECCS-1611231). A.B. and S.B. gratefully acknowledge support from the National Science Foundation (NSF) (Award No. DMR 1508603 and 1508783). R.V. and D.G. gratefully acknowledge funding from the National Science Foundation (NSF) (Award No. ECCS-1610200) and the NSF EPSCoR CIMM project (Award No. OIA-1541079).

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