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Review

Review of lateral epitaxial overgrowth of buried dielectric structures for electronics and photonics

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ABSTRACT

Integration of embedded dielectric structures with crystalline III-V materials has generated significant interest, due to a host of important applications and material improvements that are central to high performance optoelectronic devices. The core challenge is the production of high-quality crystalline layers grown above embedded dielectric materials, requiring the growth processes of both lateral epitaxial overgrowth (LEO) and coalescence. In this review article, we provide a detailed and up-to-date description of the recent advances in both LEO and coalescence in III-V materials, from its extension to molecular beam epitaxial growth and high-quality coalescence in InP and GaAs to emerging applications that utilize encapsulated air voids to enhance optical devices. We also explore the epitaxial integration of other materials, particularly metals, with III-V semiconductors.

1. Introduction

Seamless integration of embedded dielectric microstructures in III-V crystal growth is a continued area of research due to its numerous important applications to optoelectronic devices. Historically, investigation into embedded dielectric microstructures within existing crystal growth techniques was solely focused on blocking dislocations at the III-V/dielectric interface in the production of low defect high mismatch III-V metamorphic heteroepitaxy [1–3]. However, recent effort has broadened the use of embedded dielectric microstructures to enhance optoelectronic functionality, such as increasing light extraction via air voids in the III-Nitrides [4,5], site-controlling the lateral position of quantum emitters [6,7], and embedding air holes to create 2D-slab and 3D photonic crystals to enhance quantum emitters [8,9]. Moreover, high lattice mismatch metamorphics have been revisited using modern growth and fabrication approaches for dislocation blocking in a variety of material systems, resulting in low defect III-V growth on silicon [10–12].

While applications utilizing embedded dielectric microstructures in III-V materials offer much promise, the central challenge remains in embedding dielectric structures while also maintaining high-quality, low defect III-V growth. Specifically, embedding dielectric materials requires growth processes known as lateral epitaxial overgrowth (LEO) and coalescence, the formation and joining of two or more crystal fronts as shown in Fig. 1. In Fig. 1(a) and (b), the primary challenge in LEO is producing sufficiently high lateral-to-vertical growth while also limiting the formation of polycrystalline deposition on dielectric surfaces. Lateral coalescence occurs when LEO crystal fronts coalesce. Additionally, when the coalescence proceeds to return the growth front to the original substrate orientation, typically the (001) surface, this is known as planar coalescence as illustrated in Fig. 1(c).

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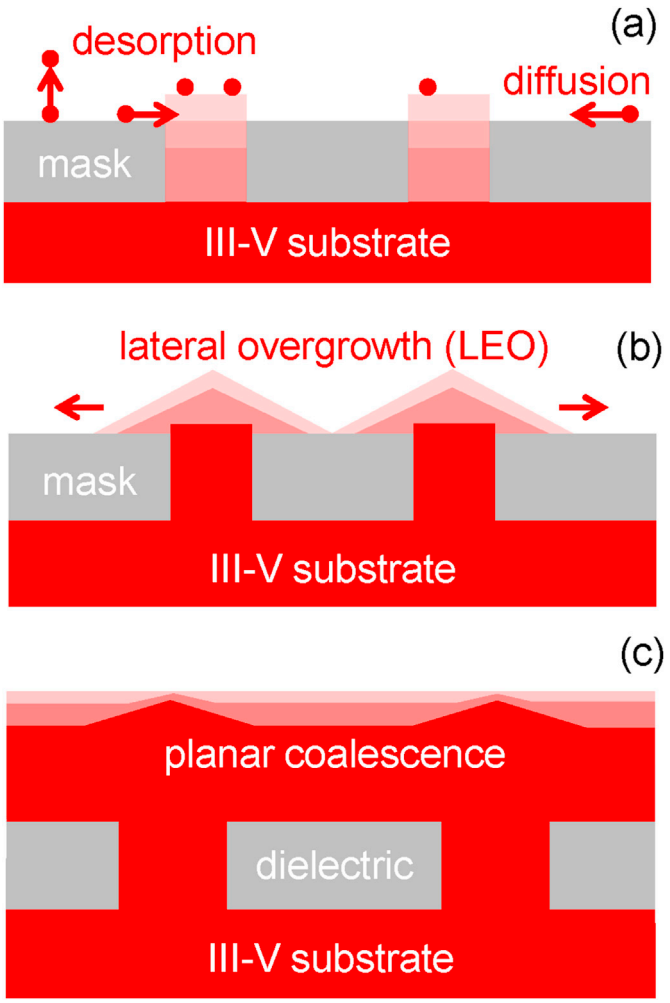

Fig. 1. Key growth events in planar coalescence growth process start by (a) maintaining selective growth, (b) producing LEO over dielectric surfaces using lateral growth techniques, and then (c) returning the growth toward a planar episurface. Adapted with permission from the American Chemical Society [13].

Although LEO and planar coalescence share common requirements in the embedding of dielectric microstructures, the quality and methodology to achieve coalescence is entirely specific to each conventional III-V crystal growth technique. As such, crystal growth technique-specific investigations for the improvement of LEO and coalescence have driven research. Since the challenges are growth-based, investigation into high-quality LEO and planar coalescence focus entirely around the methodologies of specific crystal growth techniques, dielectric microstructure geometries (typically gratings), and substrate orientation. Historically and presently, metal-organic vapor phase epitaxy (MOVPE) is the preferred lateral growth technique, owing to its vapor phase growth precursors forming limited polycrystalline nucleation on amorphous dielectric patterns like silica, thus achieving highly selective growth. Thus, the first reports of LEO with conventional III-V materials were investigated in the homoepitaxial growth of GaAs and InP using chloride VPE and MOVPE on (110) substrates [2,14,15]. In this initial work, lateral-to-vertical growth as high as 25-fold over silica and carbonized resist gratings were reported, although characterization of material quality was not reported.

From the initial MOVPE reports, greater attention to LEO including planar coalescence was explored by Nishinaga et al. using liquid phase epitaxy (LPE) growth of both homoepitaxial and metamorphic GaAs, as well as InP and GaP, over silica microstructures on (111)B and (100) oriented substrates [1,16–19]. Like MOVPE, LPE is another preferred crystal growth technique for lateral growth due to the liquid phase, which is highly selective to amorphous materials like silica [16,17,20]. Also, LPE-based LEO demonstrated exceedingly high lateral-to-vertical growth up to 50x [21]. Perhaps more importantly, mechanisms for coalescence were first established in GaAs, GaP, and InP homoepitaxial systems [17,22,23]

While use of LPE growth has diminished, recent progress using modern MOVPE, HVPE, and MOCVD growth has demonstrated high-quality homoepitaxial and metamorphic dielectric integration. Since its initial work, LEO and planar coalescence through MOVPE have been demonstrated in homoepitaxial and metamorphic systems over micron-scaled structures in a wide variety of conventional III-V systems on (001) oriented substrates [11,24,25]. Also, MOCVD has been critical in providing a more systematic understanding of

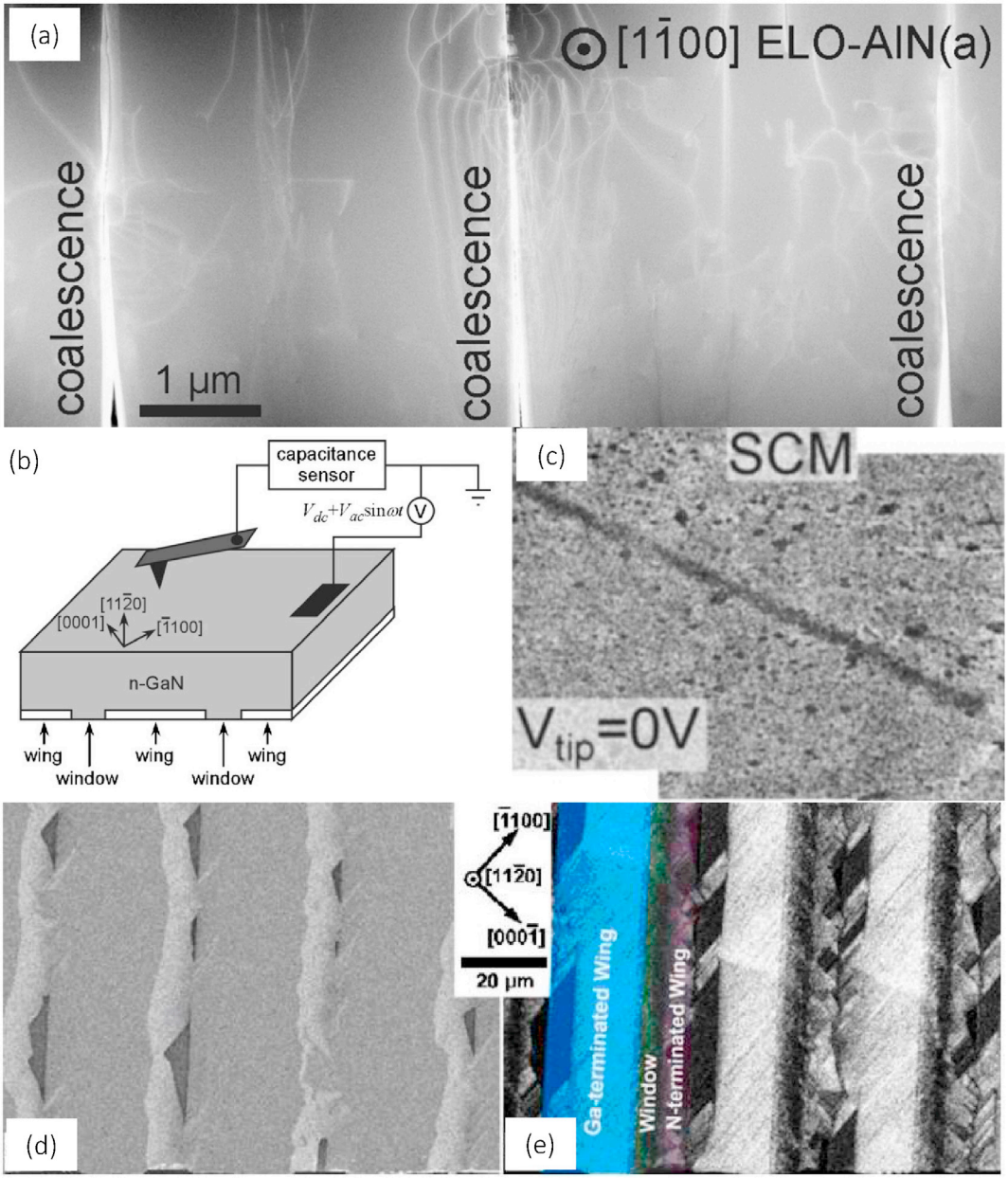

Fig. 2. (a) Cross-sectional annular dark field scanning transmission electron microscope image showing the vertical coalescence grain boundaries and threading dislocations in coalesced AlN grown by MOCVD on sapphire miscut towards the a-plane. Adapted with permission from Elsevier [33]. (b) Scanning capacitance microscopy (SCM) schematic and (c) image showing basal plane stacking fault-related electronic defects in MOVPE-grown a-plane GaN resulting from coalescence. (d) Planview SEM and (e) cathodoluminescence showing an uneven coalesced surface and nonradiative recombination sites on the same sample as (c). Adapted with permission from the Applied Institute of Physics [34].

coalescence in both homoepitaxial and metamorphic III-V systems [26,27], including planar coalescence as well as the growth for emerging applications utilizing embedded low-index photonic materials [9,28]. As discussed in-depth in Section 3, one of the challenges often encountered with LEO is the well-known "coalescence-problem." This is illustrated clearly in III-N materials grown by MOCVD in Fig. 2, which shows defect characterization in coalesced films, demonstrating the significant challenges associated with overgrowing high-quality material. For a thorough review of III-N ELO, see Hiramatsu's review [29]. Furthermore, research into understanding the growth dynamics of III-V selective area epitaxy by MOCVD has resulted in the synthesis of 2D nanostructures lacking the twin-defects and stacking faults typical of nanowire growth [30–32], suggesting a path toward the development of novel III-V device geometries.

In this paper, we will focus on the most recent advances in dielectric integration within conventional III-V growth and its device applications. In Section II, we describe the recent advances in extending LEO and planar coalescence to molecular beam epitaxy (MBE), a

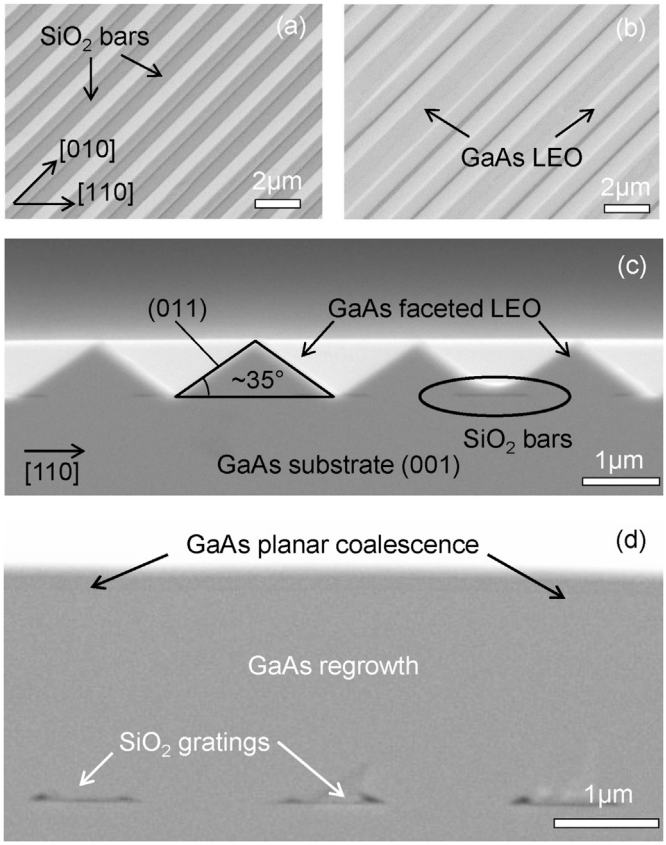

Fig. 3. Lateral growth across [010]-aligned silica grating after (a) 180 and (b) 360 cycles of periodic supply epitaxy (PSE). Cross-sectional SEM of lateral coalescence over [010]-aligned gratings. (d) Cross-sectional SEM of embedded silica gratings after planarization. Adapted with permission from American Chemical Society [13].

III-V growth technique long considered incapable of high-quality LEO and coalescence. In Section III, we detail the recent findings in homoepitaxial planar coalescence and its impact for emerging applications. In Section IV, we explore recent crystal growth techniques for embedding air nano- and microstructures for use in the emerging application of embedded high-contrast photonics. In Section V, we detail recent advances to III-V metamorphics using embedded dielectrics for defect blocking commonly coined epitaxial lateral overgrowth metamorphics or ELO as it is commonly abbreviated. And lastly, in Section VI, we discuss the extension of LEO techniques to patterned metal microstructures for full integration of semiconductors, dielectrics, and metals.

2. Extending LEO and coalescence to MBE

While prevalent in III-V crystal growth, solid-source MBE has a well-known "coalescence problem," historically lacking approaches which achieve planar coalescence over dielectric microstructures. Limited growth mechanisms for LEO and coalescence within MBE is in large part due to low diffusion of III-adatoms on dielectric surfaces, typically below 200 nm [35]. As such, growth on dielectric surfaces exceeding a diffusion length in width forms polycrystalline deposition, forcing conventional MBE growth to embed dielectric structures at the nanoscale.

To overcome this growth challenge, effort has been dedicated to extend LEO and coalescence to MBE through unconventional growth approaches. Low-angle incidence microchannel epitaxy (LAIMCE) first proposed by Nishinaga et al. is a selective MBE growth technique that enhances both lateral diffusion and selective growth by sending III and V fluxes at a low angle, fixed at 10° with respect to the substrate, leading to micron-scale LEO over dielectric masks [36–38]. While successful at achieving LEO at relatively high growth rates of 1 μm/h, this technique has many undesirable features for high-quality coalescence. At a systems level, a highly modified MBE chamber is required to orient effusion cell flux at low angles to the substrate to achieve LAIMCE results. Also, the LAIMCE technique results in the formation of screw dislocations at the joined crystal fronts when extended to lateral coalescence, making it challenging for high optical quality applications [39]. Additionally, no pathway for regaining a planar episurface has been reported using the LAIMCE technique.

Molecular beam epitaxy-based LEO can also be accomplished through the fabrication of dielectric structures below sub-adatom diffusion length scales and growth at elevated temperatures [40]. At 630°C, Ga adatom sticking coefficient on silica surfaces is less

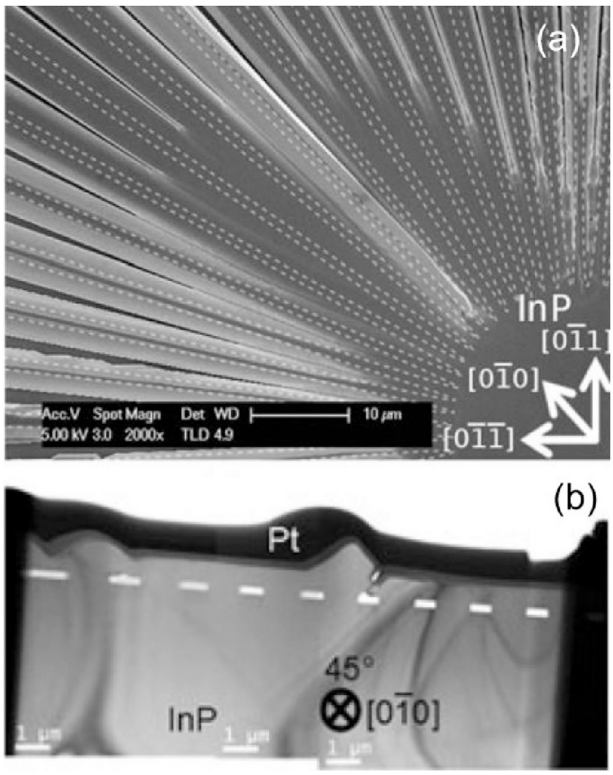

Fig. 4. (a) Planview SEM demonstrating lateral growth and coalescence dominant along the ⟨0$\bar{1}$0⟩. Adapted with permission from the Minerals, Metals and Materials Society [26]. (b) Cross-sectional TEM demonstrating high-quality embedded silica gratings in planar coalescence of InP for gratings aligned to the ⟨0$\bar{1}$0⟩. Adapted with permission from the Minerals, Metals and Materials Society [26].

than 1% of the total flux while maintaining near unity Ga sticking on GaAs surfaces. Thus, through the fabrication of nanostructures below Ga adatom diffusion length scales typically below 200 nm, poly-crystalline free growth on silica surfaces is guaranteed. As such, under tailored growth conditions, LEO was reported on silica surfaces. While successful, many aspects of this approach are undesirable, chiefly the use of nanoscale dielectric structures requiring challenging holographic lithography, limiting use to deep submicron embedded applications. Also, this work did not demonstrate a pathway toward coalescence.

The most effective approach to date for MBE LEO over micron-scaled patterns was reported by Nishinaga et al. using Periodic Supply Epitaxy (PSE) [41], a solid-source MBE growth technique using cyclic group-III deposition under a constant group-V overpressure. Periodic cycling of the group-III source limits polycrystalline formation to small nuclei on dielectric surfaces after which the periodic growth pauses allow for the decomposition and desorption of the polycrystalline nuclei off the dielectric surface. Importantly, PSE growth is able to extend Ga diffusion length on silica surfaces from 200 nm under continuous conventional MBE growth to nearly 60 μm using PSE growth approach [42], creating diffusion length scales sufficiently large for dielectric integration at the micron scale. Additional PSE experiments demonstrated highly-selective LEO over micron-scale gratings aligned to the [110] and [1$\bar{1}$0] directions, leading to non-planar lateral coalescence over the silica gratings [43]. While promising, this report only confirmed lateral coalescence via planview and cross-sectional AFM; no additional imaging or characterization of the material quality of the lateral coalescence was reported. Furthermore, a pathway toward resolving the lateral coalescence to a planar surface was not provided.

More recently, a pathway for planar coalescence over embedded dielectric microstructures using an entirely solid-source MBE approach was reported by Ironside et al. [13,44] An all-MBE approach achieved planar coalescence by developing a two-stage growth process, merging the PSE growth for LEO with self-ordered planarization of non-planar substrates to produce planar coalescence. In the first stage as seen in Fig. 3(a–c), high-quality LEO was identified for gratings aligned to the [010], forming well-faceted {011} LEO across the grating surface when using PSE growth. Limited LEO was found for [1$\bar{1}$0]-aligned gratings, as growth is preferred in the channels [45], whereas LEO occurred over [110]-aligned gratings, but occurred with multifaceted growth, leading to uneven lateral coalescence unsuitable for planarization. Then, in using the [010]-aligned gratings were used to produce a non-planar template, the growth transitioned to the second stage through tailored continuous growth to yield planarization occurring in part through the high surface diffusion of {011} facets [46], to successfully return the (001) substrate orientation as seen in Fig. 2(d). The resulting planar coalescence returned a smooth (001) surface with surface roughness as low as 3 nm root-mean-square and high optical quality. This report marked the first demonstration of planar coalescence over embedded dielectric microstructures in MBE.

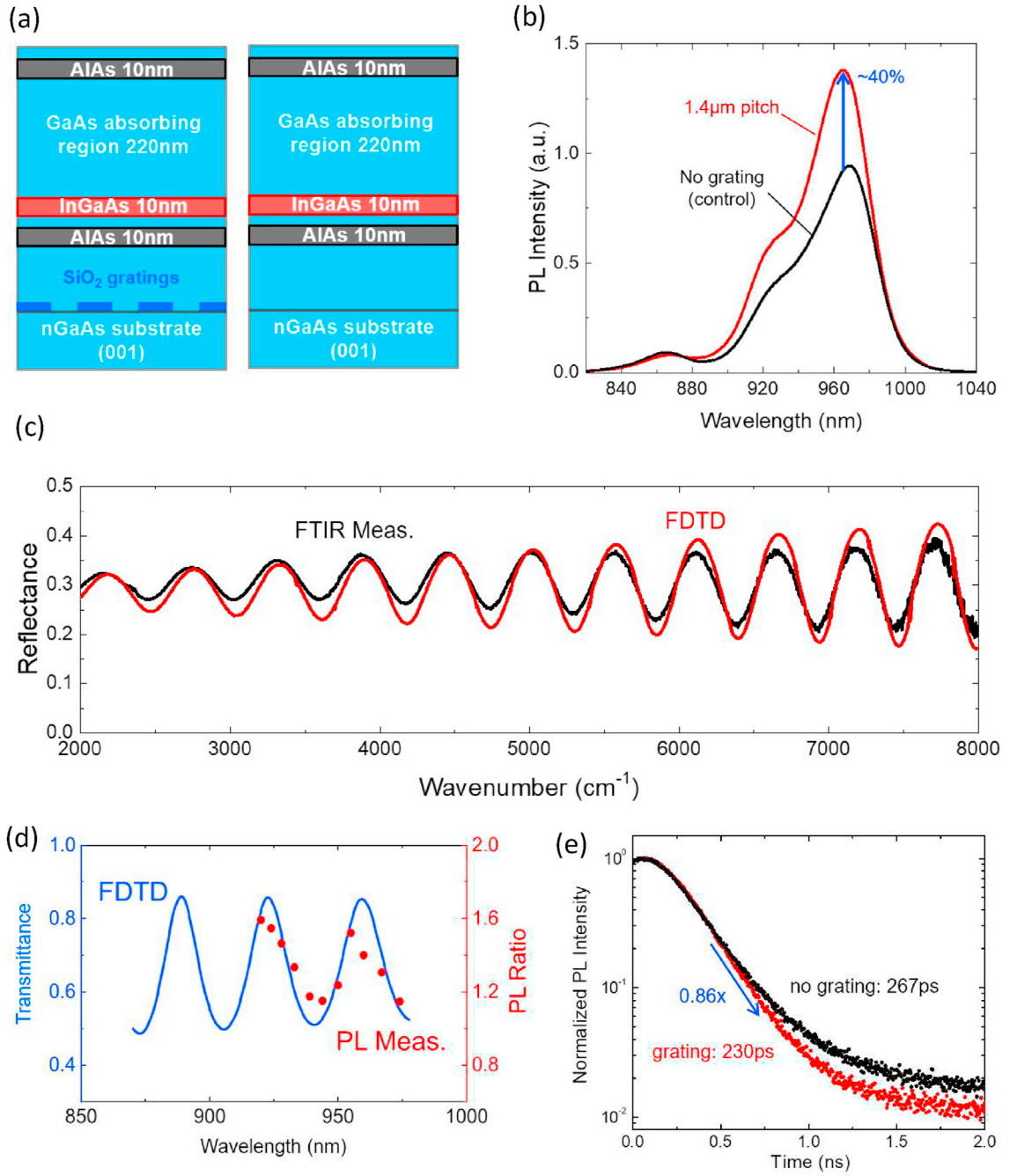

Fig. 5. (a) Layer structures for the embedded silica-enhanced quantum well and control quantum well. (b) A 1.4-fold increase was observed in room-temperature PL of an InGaAs/GaAs/AlAs emitter grown above 1.4 μm pitch $\langle 0\bar{1}0 \rangle$-aligned gratings compared to a grating-free control. (c) Fourier Transform Infrared Spectroscopy (FTIR) measurements show reflectance oscillations that agree well with full wave finite difference time domain (FDTD) modeling. (d) Enhancement was shown to be from increased extraction by comparing temperature-dependent PL with FDTD modeling, as well as (e) Purcell Effect from time-dependent PL. Adapted with permission from American Chemical Society [13].

3. Improving coalescence in III-V growth

The quality of coalescence from LEO over dielectric microstructures was first investigated by Nishinaga et al. using LPE [17,22,23]. Specifically, planar coalescence of LEO was found to have two distinct modes, each of which determined the resulting crystal quality. When crystal fronts coalesce at a singular point known as a "one-zipper" mode, no defects form as a result of the coalescence. However, when crystal fronts coalesce at more than one front, known as "two-zipper" mode, threading dislocations form at the last point of

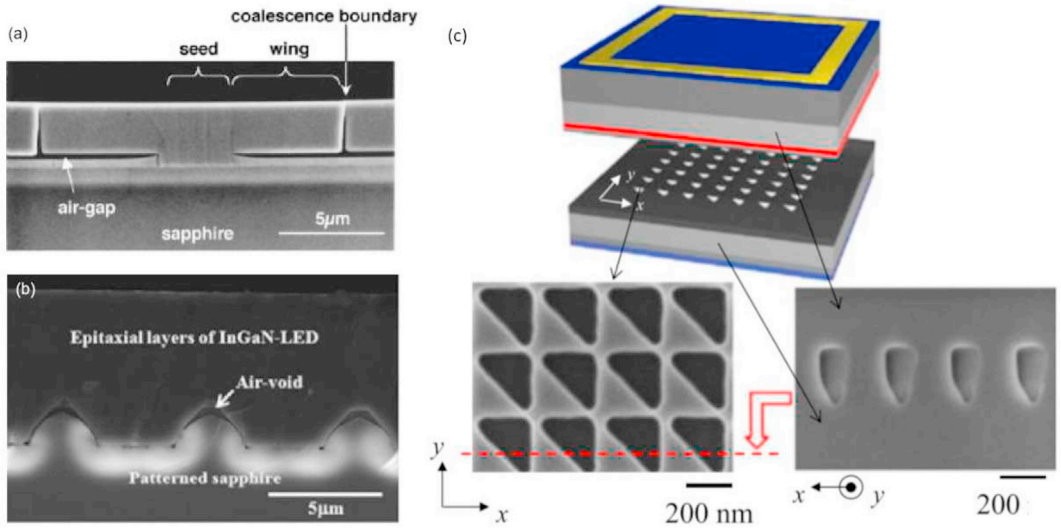

Fig. 6. (a) Air gaps form from lateral growth from pendeo-epitaxy in GaN. Adapted with permission from the American Institute of Physics [48]. (b) Patterned sapphire substrates also form air voids in GaN growth. Adapted with permission from the American Institute of Physics [49]. (c) Embedded 2D photonic crystal slabs comprised of air holes formed first by *ex situ* etch and then regrown with GaN and GaAs. Adapted with permission from the Institute of Electrical and Electronics Engineers [8].

coalescence. With respect to high optical quality applications, "two-zipper" coalescence results in exceedingly high threading dislocation densities on the order of 10^7 cm^{-2}, undesirable for optoelectronic applications.

Since the initial investigations by Nishinaga et al., recent effort has aimed to further understand and improve III-V coalescence in MOVPE and MBE growth techniques. Among recent reports, detailed investigation to planar coalescence in MOVPE growth was performed by Julian et al. [26] of homoepitaxial InP over silica gratings on (100) InP substrates. Specifically, LEO and coalescence was found to vary with V/III ratio and grating alignment to primary crystal directions. Using star-like silica patterns with orientations ranging in 5° increments in all crystal directions as seen in Fig. 4(a), coalescence was found to be most favorable along the ⟨010⟩ directions. Variation in the V/III ratio changed the position of favorable coalescence around the ⟨010⟩ directions. Transmission electron microscope (TEM) imaging also identified "one-" and "two-zipper" like coalescence modes in MOVPE growth mirroring similar investigations in LPE further controlled by the V/III ratio and grating alignment. Likewise, high-quality planar coalescence was observed for gratings aligned in the $\langle 0\bar{1}0 \rangle$ direction as seen in Fig. 4(b).

High-quality planar coalescence has also been demonstrated with MBE using a two-stage growth approach over [010]-aligned embedded silica gratings. As a means to illustrate the utility of a recently developed growth approach, Ironside et al. demonstrated that it is possible to tailor embedded structures to enhance emission of InGaAs/GaAs/AlAs quantum well (QW) test structures [13,44]. As seen in Fig. 5(b), a 1.4-fold enhancement to photoluminescence from test emitter grown directly above embedded 1.4 μm pitch silica gratings was observed compared to grating-free controls. The encapsulated grating reflectance as measured by Fourier Transform Infrared Spectroscopy was found to be oscillatory with wavelength and in close agreement with full wave finite difference time domain (FDTD) predictions as seen in Fig. 5(c). The photoluminescence enhancement in the embedded grating structure was found to have a wavelength dependence matching the reflectance measurements as seen in Fig. 5(d). The increase in PL emission was identified as emission extraction enhancement and Purcell effects. The high index contrast grating structures act as a backside mirror, with enhancements in photoluminescence demonstrating the wavelength-dependent enhancement properties of the structure. However, increases in reflectance alone do not fully account for the emission enhancement. Time-resolved photoluminescence shows a reduction in carrier lifetime for the buried grating structures as seen in Fig. 5(e), suggesting an increase in the local optical density of states that further enhances light emission from the quantum well. These studies demonstrated the enhancement of PL emission from buried dielectric structures through a seamless growth approach. This study also verified that MBE-based coalescence produced high optical quality material without significant non-radiative defects. Additionally, the high-quality coalescence observed for [010]-aligned gratings in MBE growth mirrored coalescence quality to MOVPE growth in InP at equivalent grating alignments [26].

4. Coalescence and integrated high-contrast photonics

A promising new field that intersects photonics with seamless dielectric integration in III-V coalescence is integrated high-contrast photonics, which aims to design and produce optical structures that control, enhance, and manipulate light emission in III-V optoelectronic devices. Embedded dielectric microstructures are a subset of the general field of high-contrast photonics, which at its core, uses the large difference in refractive index between two or more materials in the control of optical mechanisms. Historically, high-contrast photonic structures have been relegated to the device periphery for ease of fabrication and device integration [47].

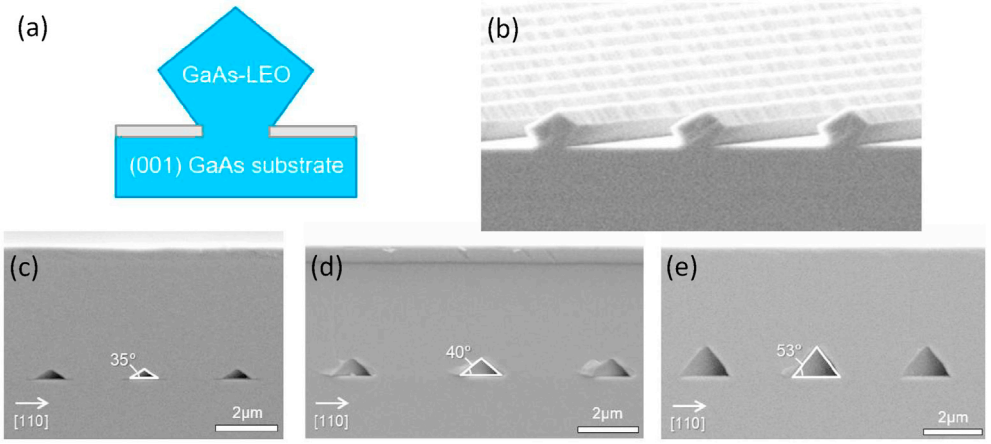

Fig. 7. (a)/(b) Inverted mesa LEO across off $\langle 0\bar{1}0\rangle$-aligned gratings in MBE growth. (c)/(d)/(e) Inverted mesa coalescence to form *in situ* air voids above the gratings at 5˚, 15˚, and 25˚ off the [010] direction.

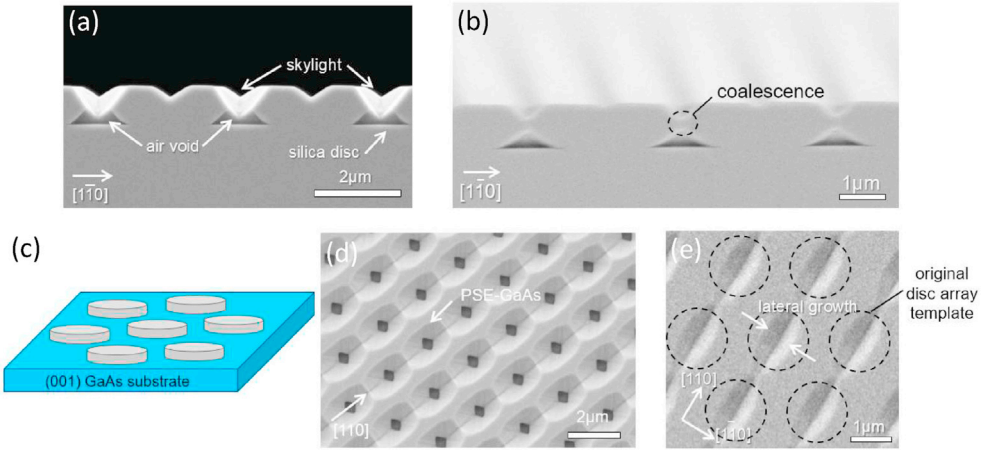

Fig. 8. (a) Cross-section of lateral coalescence above dielectric disks during coalescence and (b) after coalescence. (c) Schematic of the dielectric disk array on GaAs. (d) Planview SEM image of the lateral coalescence above dielectric disks during and (e) after coalescence.

However, with seamlessly integrated photonics as the goal, methods to encapsulate or embed low-index microstructures married with active III-V active quantum structures have become a more recent focus. While recent high-quality integration of embedded dielectric microstructures offers a path forward, full high-contrast realization is best achieved with embedded air structures. Thus, recent effort has focused on producing III-V lateral growth method to produce encapsulated air structures through coalescence.

Recent work has demonstrated use of embedded low-index photonic materials to enhance photonic and optoelectronic devices using seamless crystal growth approaches. One emerging application is to utilize embedded air voids to increase light extraction in LEDs which are fundamentally limited by total internal refraction [4,5]. Using air voids as low-index backside reflectors, emission typically lost to the substrate is redirected out the top of the device, resulting in increased net extraction efficiencies as high as 60% [4,5,50]. In the III-Nitrides, air voids can be formed by patterned sapphire substrates [49,51], patterned silica masks [52,53], selective-area Ar-implanted sapphire substrates [54,55], and pendeo-epitaxy [4,5,50,56], examples of which can be seen in Fig. 6(a) and 6(b). Void shapes are wide ranging, and generally depend on the lateral growth dynamics specific to the Wurtzite crystal structures of the III-Nitrides [3]. Embedded silica microstructures also produce similar efficiency improvements in GaN-based LEDs [57].

Embedded air voids and silica nanostructures have also enhanced laser devices [8,58]. Chief among the reports are using embedded low-index microstructures arranged 2D slab photonic crystals (PC) schemes to act as a backside mirrors or resonant cavities to enhance emission from emitters known as photonic crystal surface emitting lasers (PCSEL) [28,59]. Notable reports from Noda et al. demonstrated backside-embedded 2D PC slabs are comprised of air voids. Wafer bonding schemes have demonstrated poor device performance when attempting to produce air voids at these scales [60,61], instead requiring monolithic growth approaches to achieve embedded arrays. As such, an *ex situ* etch is first used to form air voids, then subsequent lateral growth and coalescence techniques are used to encapsulate the air voids [61–63] as seen in Fig. 7(c). Using this process, PCSEL operation has been demonstrated through MBE and MOVPE growth techniques. While promising, air hole generation demonstrated by the PCSEL technique is limited to submicron scales,

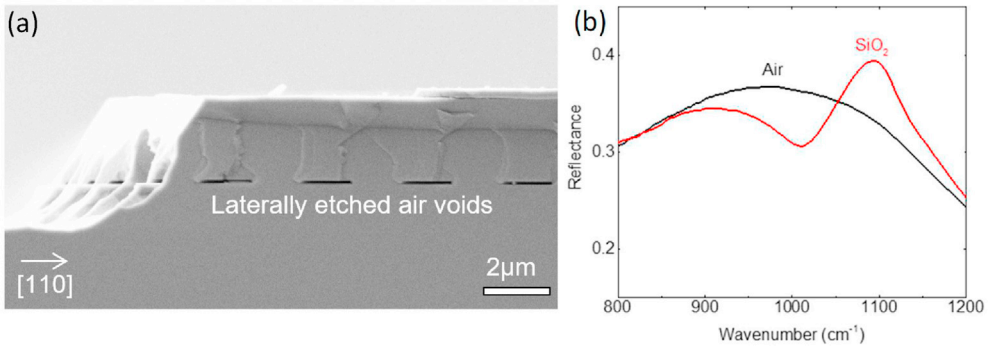

Fig. 9. (a) Air channels can be embedded using dielectric structures as a selective etch mold. (b) Reflectance spectroscopy of silica phonon resonance can be used as an indicator for etch removal of buried silica structures.

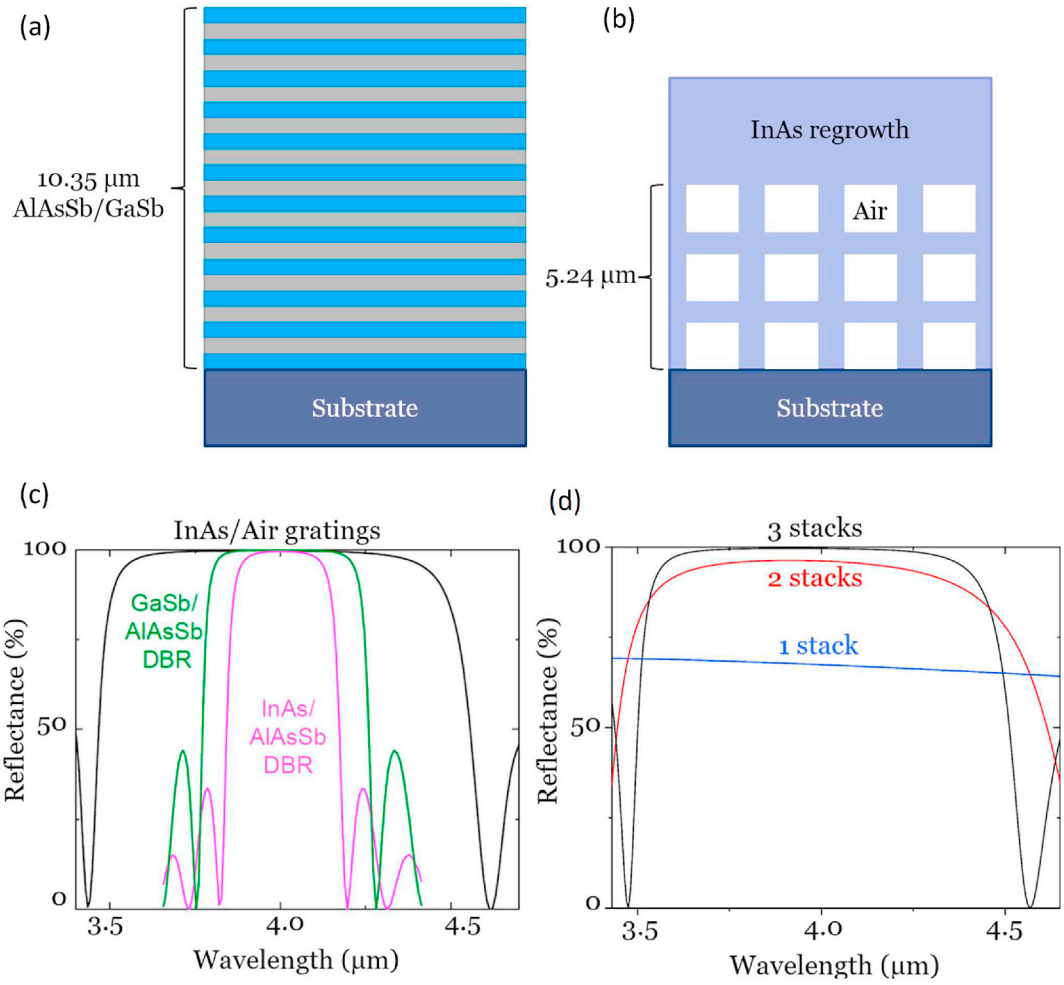

Fig. 10. (a) Layer structure of a mid-infrared distributed Bragg reflector (DBR) centered at 4 μm. (b) Layer structure of a proposed InAs/air void DBR replacement structure centered at 4 μm. (c) Rigorous coupled wave analysis (RCWA) simulation comparing conventional mid-infrared DBRs to the proposed InAs/air void structure. (d) RCWA simulation demonstrating the influence of the number of air void layers on the reflectance spectrum.

since air hole formation requires growth at sub-adatom diffusion length; thus, the process is not scalable to greater fill factors needed to extend PCSELs to the mid or near-IR.

Recently, a path for *in situ* air hole formation has been proposed by Ironside et al. using embedded patterned dielectric masks [64]. Using off-[010] aligned silica gratings, self-formed air voids formed as a consequence of inverted mesa "non-wetted" LEO specific to

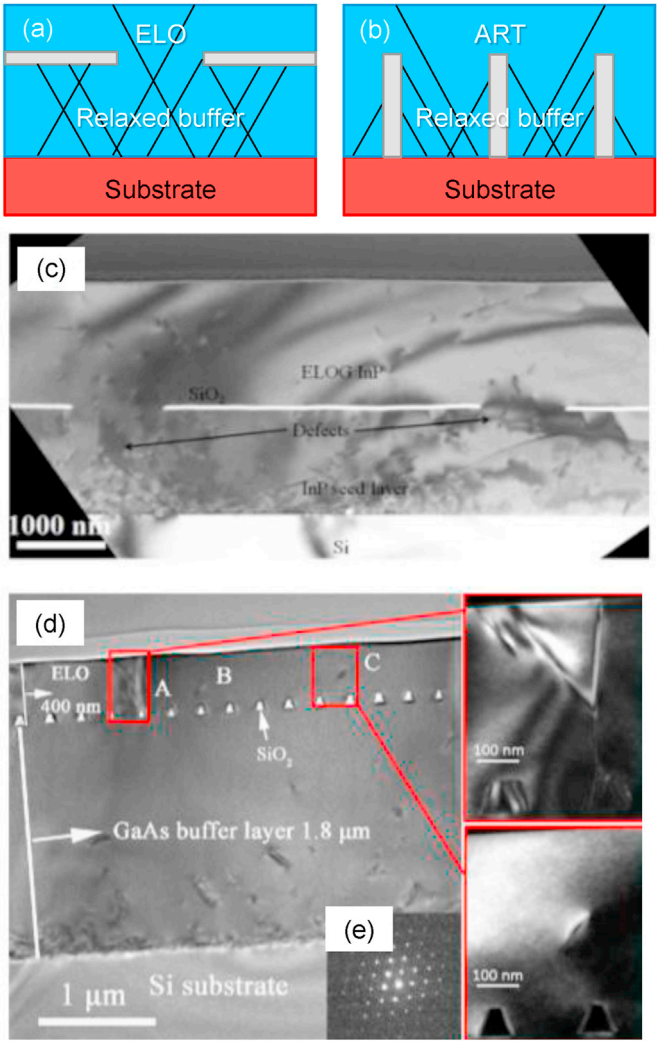

Fig. 11. (a) Epitaxial lateral overgrowth (ELO) metamorphics used thin, wide dielectric gratings or meshes to block dislocations in contrast to (b) aspect ratio trapping (ART) metamorphics which using high aspect ratio fins in heteroepitaxial conventional III-V growth. Using previously describe homoepitaxial coalescence reports, high-quality planar coalescence also extends ELO metamorphic growth on silicon substrates as demonstrated in (c) InP. Adapted with permission from the Institute of Electrical and Electronics Engineers [11]. and (d)/(e) GaAs. Adapted with permission from the American Institute of Physics [27].

grating off-primary alignment from the [010] direction toward the [110] direction as seen in Fig. 7(b). This is in contrast to lateral growth across [010]-aligned grating which were observed to have "wetted" growth across the gratings [13] as seen in Fig. 3(c). Importantly, air voids were capable of being laterally encapsulated while also regaining a smooth planar (001) substrate orientation as seen in cross-sectional SEM imaging in Fig. 7(c)–7(e). Depending on the degree of alignment between the [010] and [110] directions, embedded air voids comprised of (011) and (111)A facets, offering some degree of tunability in void angle depending on the specific grating alignment. As a natural extension, air voids of mixed (011) and (111) can be encapsulated above non-grating dielectric masks. Specifically, Ironside et al. also showed the formation of rhombic pyramidal structures above hexagonal arrays of silica disks comprising of a superposition of (011) and (111) type facets as seen in Fig. 8. Since lateral growth is not fixed to primary crystal directions as in gratings, disk arrays form air voids comprised of preferred lateral growth direction around the [010] direction. Similarly, using a two-stage MBE growth process, air voids achieve both lateral encapsulation and planar coalescence. For homoepitaxial systems, the planar coalescence over encapsulated air voids occurred at equivalent optical quality compared to dielectric-free controls and episurface roughness below 3 nm root-mean-squared (RMS).

While the triangular shape of self-formed air voids is fixed largely by the underlining zincblende crystal structure of conventional III-V alloys, an arbitrary embedded air void approach was recently demonstrated using colloidal dielectric spheres as an etch mold to create epitaxially buried 3D photonic crystal arrays in GaAs [9] and GaInP [65]. More specifically, embedded silica spheres are sufficiently dissimilar from conventional III-V materials to produce a highly selective etch using HF or buffered oxide etch (BOE). By prepatterning silica opal spheres, selective growth at the nanoscale was achieved using MOCVD and HVPE crystal growth by seeding epitaxial growth

from the substrate through the open portions between the spheres. Once the growth is completed, a post-growth *ex situ* selective etch removes the dielectric spheres, leaving behind air voids and producing high-contrast 3D photonic crystal arrays. Likewise, in regaining an epitaxial surface, growth of active III-V structures, including electrically pumped LEDs [9], were shown to be optically coupled to the buried 3D photonic material.

A similar strategy was also developed by Skipper et al. using embedded dielectric gratings as a mold to produce air channels after post-growth selective etching [66]. Silica gratings can be integrated using suitably tailored growth, then once embedded, III-V is etched back down to the grating level, and then removed laterally using a highly selective wet etch. Demonstration of the process using BOE was shown in GaAs for gratings as thin as 0.7 μm by 0.1 μm as seen in Fig. 9(a). Confirmation of the depth of the lateral etch was determined using the phonon resonance near 10 μm in FTIR reflectance spectroscopy as seen in Fig. 9(b), with lateral etch depth as far as 200 μm for an etch rate of approximately 20 μm/h to be used at device scales.

Lastly, due to the challenging production of embedded dielectric media in III-V crystal growth, many device designs remain theoretical at present. Some interesting applications using embedded low-index microstructures in III-V media include guided mode resonance for embedded optical filters [67–69], embedded low-index structures for backside all-dielectric broadband mirrors [70,71] and active III-V emitters coupled to embedded waveguides using an integrated photonic circuit approach [72]. As seen in Fig. 10, simulations predict that the high index contrast between III-V semiconductors and air enable the fabrication of mid-infrared mirrors that are simultaneously thinner and broader band than conventional distributed Bragg reflectors. Thus, from the multitude of recent theoretical and experimental reports, it demonstrates the potential impact of embedded low-index microstructures to active III-V optoelectronic devices.

5. Using embedded dielectrics for ELO metamorphics

With high-quality heterogeneous layers as the goal, one of the primary objectives is to relax large lattice-mismatches to produce high-quality metamorphic buffers with reduced defect densities in the surface device layers. While a great deal of progress has been made to relax a wide array of binary high lattice mismatch III-V alloys on Si and GaAs substrates [73], the common trend is the generation of exceedingly high densities of threading dislocations, greater than 10^8 cm^{-2}, even when thick buffer layers are employed. Several growth methods to reduce threading dislocation propagation in relaxed metamorphic buffer layers have been proposed such as graded buffer layer schemes [74,75], strained superlattice dislocation filters [76–78], and compliant substrates [79,80]. One technique that has shown great promise with high lattice mismatch metamorphics is epitaxial lateral overgrowth heteroepitaxy or ELO as it is commonly abbreviated. In the ELO technique as illustrated in Fig. 11(a), patterned dielectric microstructures, typically gratings or meshes, block threading dislocation propagation at a former growth front while also incorporating periodic openings commonly referred to as windows to seed lateral growth across the dielectric microstructures. Therefore, performing high-quality lateral growth and coalescence produces regions directly above the dielectric microstructures with limited threading dislocations, ideally only allowing threading dislocations placed near the seed window openings to continue propagation.

ELO metamorphics as described here are not the only embedded dielectric technique used for a dislocation blocking. One other notable technique is aspect ratio trapping (ART) [10,81,82]. As illustrated in Fig. 11(b), ART utilizes patterned high aspect ratio fins to block dislocation propagation at the vertical dielectric interface in contrast to ELO which uses horizontal patterns at low aspect ratios to block dislocation propagation. While both techniques can be highly effective, ART benefits from integration in a single epitaxial growth step with the challenge of fabricating tall dielectric fins at a very high aspect ratio using unconventional nano-patterning whereas ELO has relatively straightforward conventional micron-scale dielectric grating fabrication but requires at least two separate growth steps. Going forward, this review will solely focus on the ELO technique.

As addressed throughout the previous section, the challenges associated with achieving ELO metamorphics, namely high-selective lateral growth and coalescence are specific to particular crystal growth techniques. As such, ELO metamorphic integration within crystal growth closely mirrors the success with homoepitaxial dielectric integration, previously demonstrated within MOVPE and LPE crystal growth techniques. Since the III-N materials have a long history of ELO due to early work in growing GaN on sapphire [83], this section will focus on the conventional zincblende III-V materials and recent integration techniques for all III-Vs with Si. For a detailed description of III-N ELO, see Hiramatsu's review [29]. In conventional III-V materials, metamorphic ELO was first performed by LPE with the growth of GaAs on (111) silicon substrates, and later InP on (001) silicon substrates [1,19,84]. While successful at producing significant LEO with low defect density above dielectric regions and demonstrating III-V/silicon integration, the growth process was not singular, requiring initial MOCVD or MBE growth to produce relaxed III-V buffer layer on silicon. Also, unlike the homoepitaxial LPE growth which demonstrated planar coalescence, no lateral or planar coalescence in LPE ELO was reported.

Since the LPE reports, more recent investigation through MOVPE has extended ELO metamorphics to a wide variety of III-V systems. ELO InP is the most common studied system in MOVPE and MOCVD, metamorphically grown on (001) GaAs [85,86] and (001) Silicon substrates [11,87–89]. A more in-depth approach to understanding coalescence quality in metamorphic InP was provided by Julian et al. using homoepitaxial InP coalescence as a comparative control [87]. More specifically, using this methodology, stacking faults identified with planview and cross-sectional TEM associated with ELO planar coalescence were able to be identified originating from the initial relaxed buffer layers rather than the coalescence itself as seen in Fig. 11(c). Importantly, this suggested that ELO methodology for dislocation blocking has the potential for great impact as the coalescence does not introduce additional defects during growth. Additionally, PL using multi-QW structures on InP was able to demonstrate ELO-InP/silicon integration within a factor of 2 of the intensity of equivalent InP homoepitaxial controls [11].

Beyond InP, ELO without coalescence was extended to GaSb on (001) GaAs substrates demonstrating dislocation reduction of silica stripes [90]. ELO with lateral coalescence was extended to InAs on (001) GaAs substrates, demonstrating grain boundary free lateral

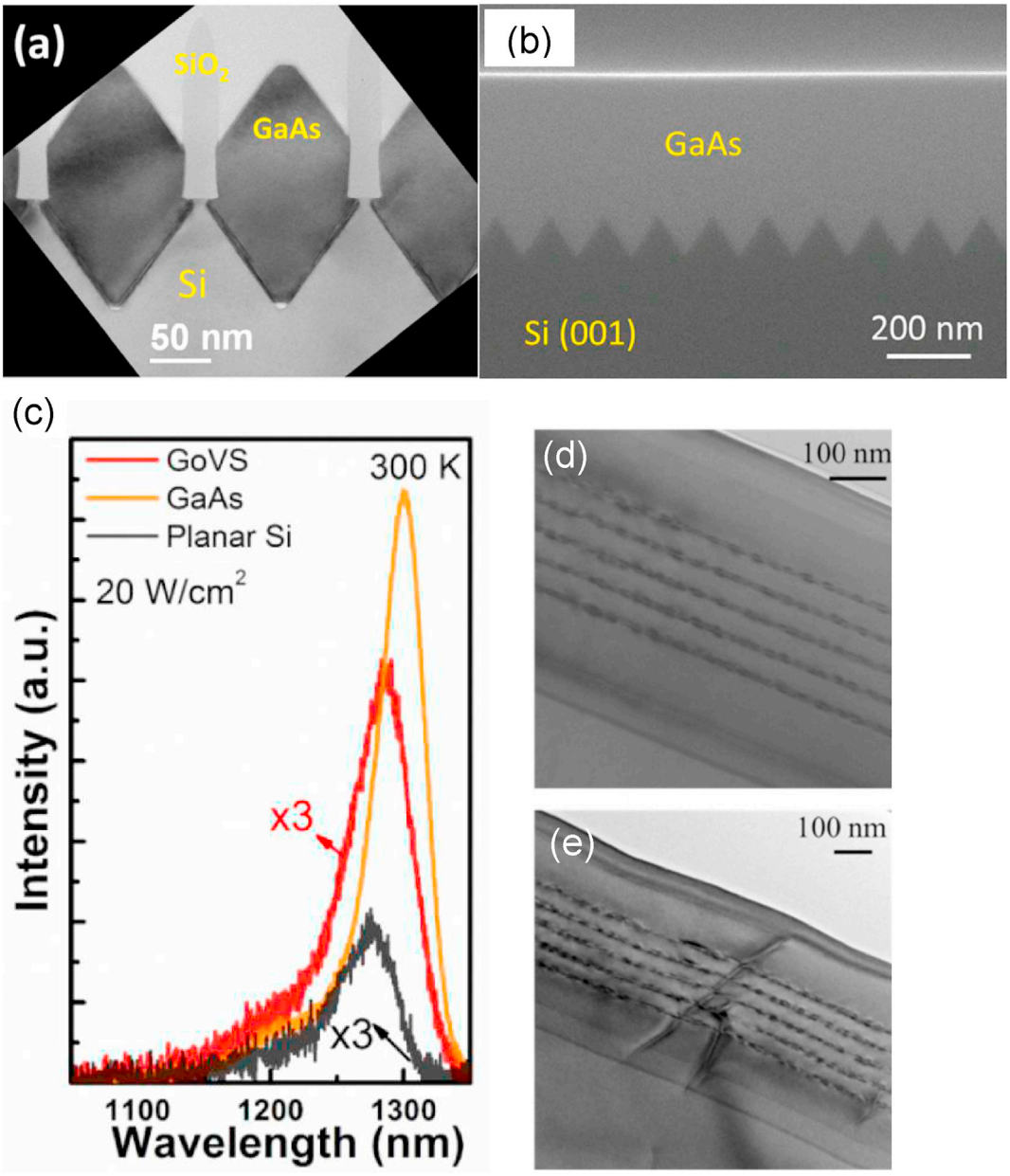

Fig. 12. (a) Cross-sectional TEM image of GaAs grown in V-grooved Si between SiO2 stripes. Adapted with permission from the American Institute of Physics [93]. (b) Cross-sectional SEM image of planarized GaAs on V-grooved Si with the SiO2 stripes removed [93]. (c) Comparison of the photoluminescence intensity of InAs quantum dots grown on planar Si, V-grooved Si, and GaAs [94]. Cross-sectional TEM image of InAs quantum dots grown on (d) V-grooved Si templates and (e) planar Si. Adapted with permission from the Optical Society [94].

coalescence when employing submicron windows and dislocation reduction below 10^7 cm^{-2} [91] Also, ELO InGaAs without coalescence was extended to (111) silicon substrates, demonstrating 10-fold vertical-to-lateral growth rate ratio over 2 μm diameter regions [92].

Metamorphic coalescence of GaAs was also investigated by MOCVD on 4° miscut (001) silicon substrates by He et al. [27]. A three-stage growth process was developed for embedding silica gratings at the submicron scale comprising of selective lateral overgrowth, coalescence, and planarization as seen in Fig. 11(d). By systemically investigating grating alignments with primary crystal directions, the [410] direction was found to produce the smoothest films at 6 nm RMS and optical quality exceeding the unpatterned GaAs/Si buffer.

In order to avoid the challenges of coalescence and achieve high-quality growth with on-axis Si substrates, Li et al. developed a process in which the dielectric is selectively removed after seeding growth on a V-groove template [93]. By utilizing an SiO2 stripe

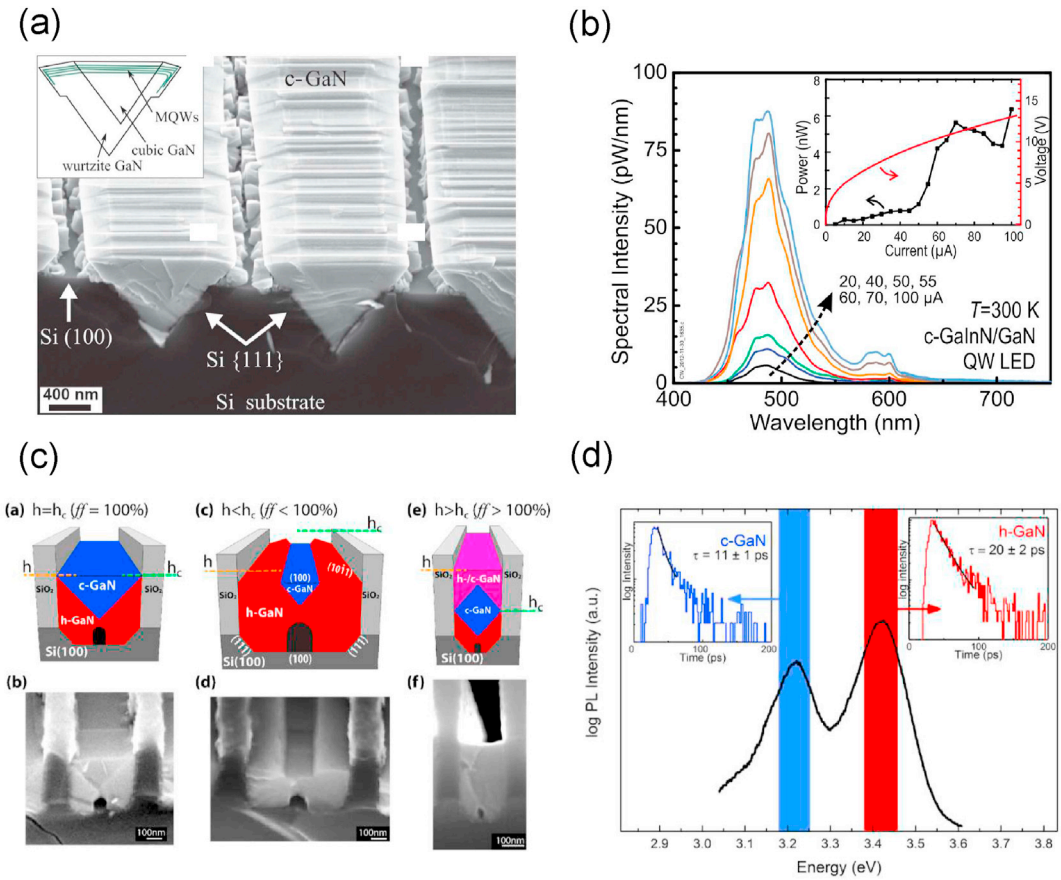

Fig. 13. (a) Cross-sectional scanning electron microscope (SEM) images of cubic GaN and InGaN quantum wells grown on grooved silicon with a schematic inset [98]. (b) Electroluminescence from the quantum well structures from (a). Adapted with permission from the American Institute of Physics [98]. (c) SEM images and corresponding schematics showing the optimization of the phase transition between wurtzite and cubic GaN with SiO2 sidewalls [99]. (d) Room temperature photoluminescence and time-resolved photoluminescence of the structures shown in (c). Adapted with permission from the American Chemical Society [99].

pattern, V-grooves with (111) facets can be etched into an (001) Si substrate. This results in a "tiara" structure at the peak of the Si ridges that traps stacking faults in selectively grown GaAs nanowires grown in the V-grooves. The SiO2 sidewalls can subsequently be removed by selective etching, allowing another growth step to planarize the GaAs surface without concern for coalescence above high aspect ratio dielectric features. These GaAs on V-groove Si templates have been used for the growth and fabrication of InAs quantum dot-based lasers [94,95] and photodiodes [96], demonstrating great promise for the integration of active III-V optoelectronics on Si without wafer bonding. As seen in Fig. 12, device structures grown on the V-groove templates show improved photoluminescence as well as a threefold reduction in threading dislocation density over growth on planar Si. By combining the V-groove Si template with a strained layer superlattice, a threading dislocation density of 5.8×10^6 cm^{-2} was achieved in the active region of an InGaAs quantum dot photodetector [97], resulting in a significant reduction in dark current.

Growth on grooved Si can similarly be used to control the crystal phase of MOCVD-grown GaN for high-performance electronic and optoelectronic devices [100,101]. Cubic zincblende GaN lacks the piezoelectric polarization fields that reduce the radiative efficiency of hexagonal wurtzite GaN-based optoelectronics, and possesses further advantages in electron mobility and p-type doping, making it an ideal candidate for device integration with silicon [98,99]. Hexagonal GaN growth is seeded from two opposite Si{111} facets in the valley of a V-groove. The coalescence of the two growth fronts results in a phase transition to cubic GaN, allowing for the growth of cubic GaN stripes on Si substrates as seen in Fig. 13 [100,101]. InGaN quantum wells grown on these GaN stripes show great promise in room temperature optoelectronics, particularly in green LEDs, which greatly benefit from the narrower band gap and lack of polarization fields compared to devices grown on conventional wurtzite GaN [98,99,102]. The addition of SiO2 sidewalls to laterally confine growth has resulted in further optimization of the cubic phase surface coverage, material quality, and radiative efficiency [99,103]

The integration of III-V semiconductors with planar unpatterned silicon and silicon-on-insulator substrates has also been enabled through lateral growth over three-dimensional dielectric templates. This technique, commonly called confined epitaxial lateral overgrowth (CELO) or template-assisted selective growth (TASE), uses dielectric channels as a mold, allowing III-V precursors to diffuse through an opening and grow nanostructures that conform to the shape of the dielectric. As seen in Fig. 14, abrupt changes in the growth

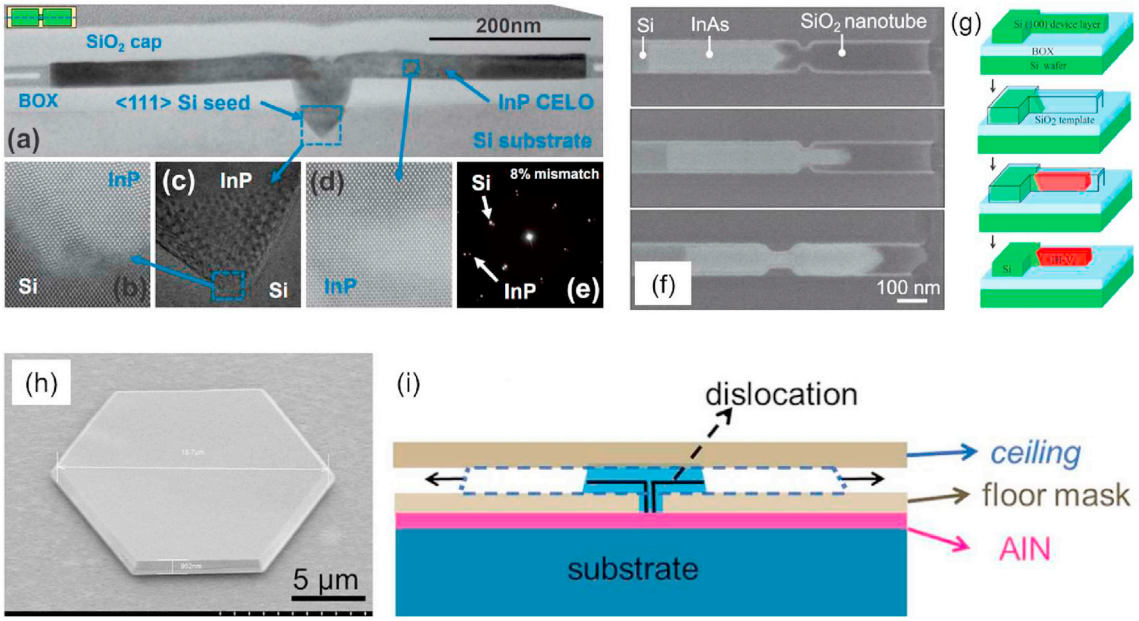

Fig. 14. (a) Cross-sectional TEM image of confined InP growth on Si with an SiO2 template [104]. (b)–(d) Cross-sectional TEM images showing the evolution of the InP crystal from highly defective at the interface with Si to a uniform lattice in the lateral overgrowth region [104]. (e) Selected area electron diffraction pattern demonstrating that the InP exhibits an 8% lattice mismatch with Si, indicating a fully relaxed layer [104]. Adapted with permission from IEEE. (f) SEM images demonstrating the growth of InAs through an SiO2 nanotube over time [105]. (g) Schematic illustrating how the nanotube template in (f) was fabricated by back-etching Si through a conformal oxide layer [105]. Adapted with permission form the Applied Institute of Physics. (h) SEM image of a large-area GaN tile seeded from growth on a Si (111) substrate using an SiO2 floor and ceiling mask as shown in (f) [106]. Adapted with permission from Wiley.

direction cause the dislocations formed at the Si/III-V interface to terminate on the dielectric template [104]. This results in the formation of high-quality planar layers of III-V semiconductors on Si or SOI substrates without buffer layers that can be used for active electronic and optoelectronic devices. However, care must be taken to optimize the size and location of the highly defective seed region to avoid interaction with device regions. TASE can also be used to create III-V nanostructures co-planar with Si as seen in Fig. 14(f) and g. By seeding growth from the sidewall of patterned Si and confining the growth to a hollow SiO2 nanotube, heterogeneous nanowire devices have been fabricated with InAs and InGaAs [105]. However, without the sharp bends of vertically seeded TASE, threading dislocations can still propagate along the nanowire axis, as illustrated schematically in Fig. 14(i). Horizontal GaN stripes have also been demonstrated [107,108], potentially enabling applications in power electronics and visible optoelectronics. GaN TASE growths have also demonstrated resiliency to wafer bowing, suggesting TASE as a pathway for integration with large-area Si CMOS production wafers [106]. Recent work in optimizing the template geometry to improve thickness non-uniformity above the seed region shows great promise for scaling TASE for novel devices in the future [109].

Lastly, ELO metamorphics was recently extended to MBE growth. Ironside et al. demonstrated threading dislocation reduction by over 3x in the InAs/GaAs system [110]. Using the recently developed two-stage growth process for GaAs [13], an equivalent growth process was developed and extended to metamorphic InAs, demonstrating highly-selective lateral growth and planar coalescence over [010]-aligned silica gratings when patterned on relaxed InAs/GaAs using the interfacial misfit array (IMF) technique as seen in Fig. 15(a) [111,112]. Threading dislocation reduction was confirmed by electron channeling contrast imaging (ECCI) measurements corroborated by an over 50% increase in PL compared to grating-free InAs/GaAs controls for 68% fill factor embedded gratings as seen in Fig. 15(b) and (c). Also, surface roughness of the InAs-ELO films were minimized to 5 nm RMS, roughly 2x greater then InAs/GaAs control.

6. Extension to patterned metal overgrowth

While the epitaxial integration of semiconductors and dielectrics has progressed rapidly in recent years, the monolithic integration of patterned metal structures with crystalline semiconductors has been comparatively underexplored. Epitaxially-embedded patterned metals could be useful in a wide variety of photonic and electronic devices to introduce both passive (e.g. polarizers or plasmonic waveguides), and active (e.g. buried Ohmic contacts) functionality. Monolithic integration of semiconductors, dielectrics, and metals would allow for 3D integration of optoelectronic devices and photonic integrated circuits. However, the integration of metals with semiconductor epitaxy presents a number of metallurgical challenges. At the elevated temperatures necessary for growth, metals can react with the semiconductor, distorting the crystal structure and forming unintentional contact spikes [116,117]. Furthermore, similar to dielectric overgrowth, the growth parameters must be carefully tailored to prevent polycrystalline deposition, as well as voids and

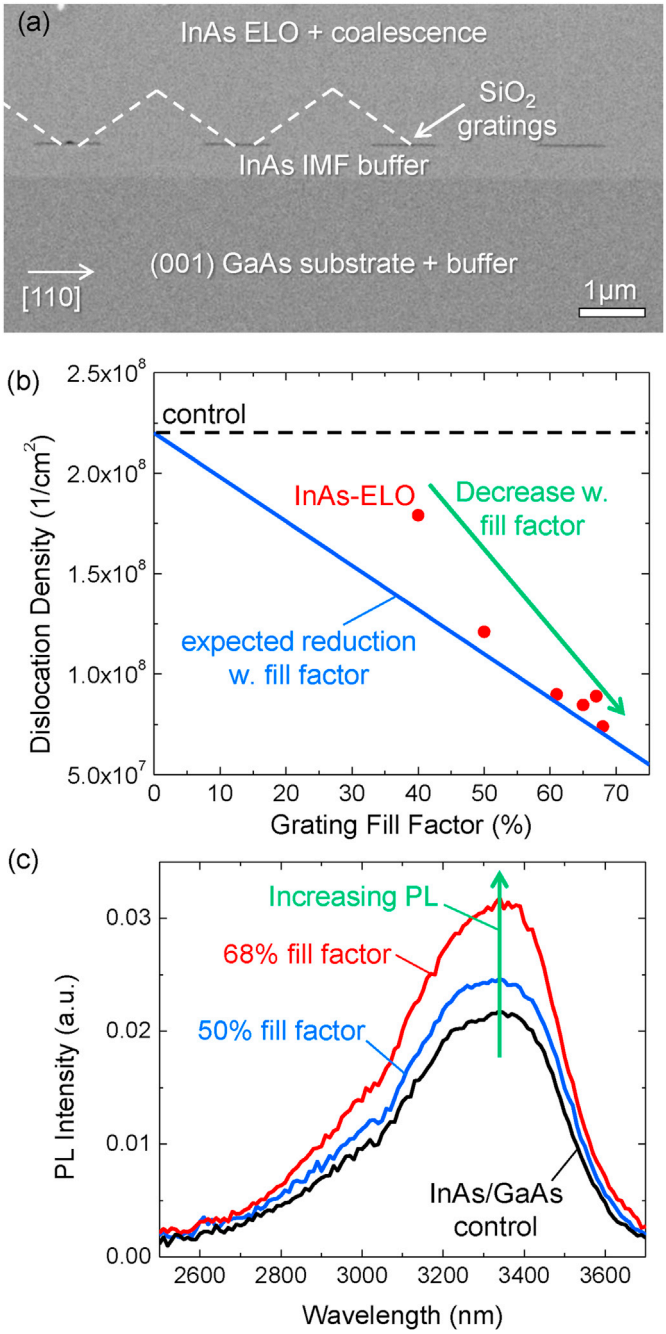

Fig. 15. (a) Using the two-stage growth process, ELO was extended to all-MBE growth in InAs/GaAs systems. (b) Using electron channeling contrast imaging (ECCI) to count threading dislocations, an up to 3x reduction in dislocation density was found in InAs-ELO compared to grating-free InAs/GaAs controls. ECCI measurements courtesy of the Minjoo Larry Lee group at the University of Illinois Urbana-Champaign. (c) Dislocation reduction was also confirmed in PL, achieving a 50% improvement in InAs-ELO PL compared to control.

dislocations which could introduce optical scattering and recombination sites that reduce the efficiency of epitaxially integrated devices.

To date, the most successful approach to integrate metals into epitaxial layer stacks has focused on rare earth pnictide (e.g. ErAs) films [118] and nanostructures [119] with applications to tunnel junctions [120–122]. For a recent thorough review of this field, please see Bomberger et al. [123] However, the self-assembled growth of rare earth pnictides makes the integration of arbitrary shaped metals challenging. Work on the integration of patterned metals by MOCVD [113,114,124], LPE [115,125], and MBE [126] has focused on tungsten due to its stability at high temperatures and non-reactivity with conventional III-V semiconductors [127]. Epitaxial lateral overgrowth of tungsten gratings has shown similar properties to the overgrowth of silicon dioxide with high dependence on crystal

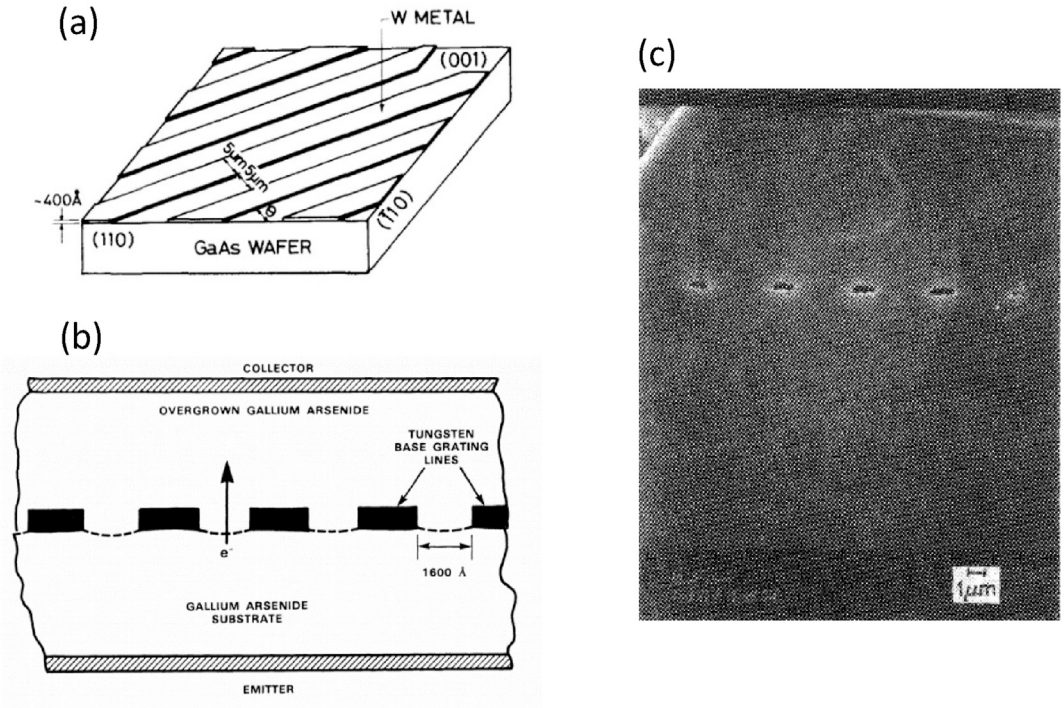

Fig. 16. (a) Illustration of the tungsten grating template overgrown by MOCVD. Adapted with permission from the American Institute of Physics [113]. (b) Illustration of the permeable base transistor design cross-section using tungsten gratings embedded in GaAs. Adapted with permission from the Society of Photo-Optical Instrumentation Engineers [114] (c) Cross-sectional scanning electron microscope (SEM) image of tungsten gratings embedded in GaAs. Adapted with permission from the American Institute of Physics [115].

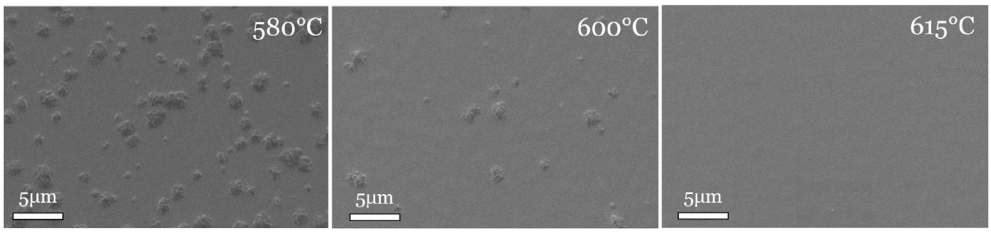

Fig. 17. Scanning electron microscope (SEM) images of tungsten surfaces after 50 nm of GaAs was grown by the PSE growth technique. Polycrystalline deposition is suppressed at higher growth temperatures, suggesting a pathway to lateral epitaxial overgrowth of metals and dielectrics by MBE.

plane orientation and growth temperature. This allowed for electronic devices such as permeable base transistors to be fabricated based on this tungsten grating overgrowth process as seen in Fig. 16. However, due to the focus on electronic devices, the optical properties of integrated metals have been largely unexplored.

Moving forward, combining epitaxially integrated dielectrics and metals would allow for the design of three-dimensional optoelectronic integrated circuits. Due to the similar requirements for overgrowing metals and dielectrics (see Fig. 17), integration with III-Vs can theoretically be achieved simultaneously for both material systems. This provides numerous options for optical gain, waveguiding, mirror design, polarization control, and modulation that can be scaled vertically as well as laterally. By further optimizing the growth space and working towards integration of metals and dielectrics in a single layer stack, epitaxial lateral overgrowth has the potential to enable a host of new photonic devices.

7. Conclusions and outlook

Recent advances in high-quality coalescence in homoepitaxial and metamorphic conventional III-V systems using CVD and MBE crystal growth techniques open up a wide new array of optoelectronic and photonic material systems to explore. Even with recent breakthroughs, much of the lateral regrowth/coalescence properties and growth space optimization remain largely unexplored outside InP, GaAs, and GaN binary alloys. This affords great opportunities for further breakthroughs. Also, demonstration of high-quality

integration of silica and air voids, gratings, and channels opens an underdeveloped design space of novel photonic systems which can couple active quantum structures for both scientific and engineering applications without limitation from defective material growth. Similarly, exciting opportunities are expected to emerge as the integration with patterned metals continues to progress. Based on the high-quality demonstrations in lateral growth and coalescence presented here, these techniques will produce further advances both in material science and photonic devices moving forward, seamlessly merging semiconductors, dielectrics, and metals.

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