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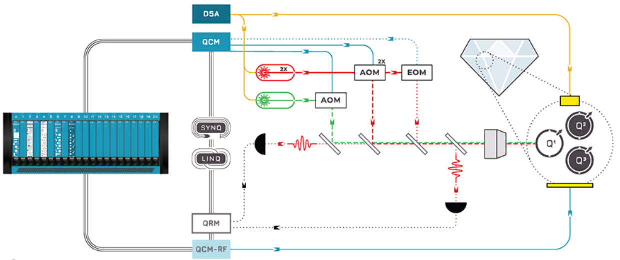

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ABSTRACT

By utilizing the low-noise benefits of staircase avalanche photodiodes (APDs) and the high-field tolerance of conventional APDs, a "cascaded multiplier" device has been grown and characterized showing significantly reduced excess noise compared to $k \sim 0$ materials. Because it can withstand higher electric fields than a pure staircase APD, the gain values are not limited by the number of staircase steps in the device, and higher gains are demonstrated. In addition, the cascaded multiplier device shows reduced dark current to staircase devices of similar gain. Slight adjustments to the device design could increase the gain to even higher values—further improving the signal-to-noise ratio in the detector.

Near- to mid-infrared applications, such as LIDAR, telecommunications, and imaging, often rely on avalanche photodiodes (APDs) for high sensitivity optical detection.[1] APD sensitivity generally trends with the signal-to-noise ratio (SNR), which, owing to internal gain from impact ionization signal multiplication, has been shown to be larger than traditional photodiode detectors.[2] Unfortunately, impact ionization is a stochastic process leading to gain variation that manifests as a contribution to detector shot noise and limits APD speed and sensitivity.[3,4] This gain variation is usually parameterized using the excess noise factor, *F(M)*, of the amplification material and is related to the impact ionization ratio between electrons and holes, *k*, by

$$F(M) = kM + (1 - k)(2 - 1/M), \tag{1}$$

where M is the internal multiplication gain of the detector.[5] The excess noise factor increases with increasing M but increases more slowly for lower values of k, leading to both improved speed and sensitivity if an APD is to operate with a substantial gain. Bulk materials, such as $Hg_{1-x}Cd_xTe$, Si, and InAs, work well as extremely low-noise amplifiers due primarily to their $k \sim 0$ characteristic.[1,6,7] Aside from bulk materials, some APDs use impact ionization engineering to achieve low noise multiplication, where band-engineered heterojunctions incentivize single-carrier impact ionization.[1]

$Al_xIn_{1-x}As_ySb_{1-y}$ (henceforth referred to as AlInAsSb) grown as a digital alloy lattice-matched to GaSb substrates has recently shown great promise for APDs in the near- to mid-IR owing to its flexible bandgap engineering, small valence band offsets, and very low impact ionization ratio, k.[8–11] For example, AlInAsSb was used to demonstrate wavelength-flexible separate absorption, charge, and multiplication (SACM) APDs with $k \sim 0.01$ performance and gain >50 and >100 at room temperature under 1.55- and 2-μm illumination, respectively.[12,13] In addition, AlInAsSb was used to demonstrate Capasso's staircase APD,[14,15] which utilizes complex alloy "step" gradings to promote deterministic, localized electron-initiated impact ionization with $\sim 2^N$ gain scaling, where N is the number of staircase steps.[16] The three-step staircase APD features a modest gain of ~ 8 and shows extremely low-noise amplification *well below* that of an ideal McIntyre-limited $k = 0$ material.[17]

Unlike a conventional APD that exhibits exponential gain with increased electric field, staircase APD gain is limited by the number of steps. Further biasing of staircase devices leads to increased dark current density due to band-to-band tunneling in the narrow bandgap staircase layers. This effect is detrimental to staircase APD operation and limits the external bias that can be applied. By leveraging the exponential nature of high-field impact ionization found in conventional

APDs, this study attempts to improve detector sensitivity by increasing the maximum gain of a staircase device. Furthermore, a high-field staircase device should decrease carrier transit times which would increase bandwidth compared to a pure (low-field) staircase APD of equal gain.[18] The SNR of a high-field staircase device would benefit significantly by using a low-noise staircase step *before* a conventional, high-field, avalanche bulk multiplier. Friis cascaded amplifier noise theory highlights the importance of the early noise contributions in a multi-stage amplifier represented by

$$F_{total} = F_1 + \frac{F_2 - 1}{M_1} + \cdots + \frac{F_N - 1}{M_1 M_2 \ldots M_{N-1}}, \qquad (2)$$

where F_N and M_N are the excess noise factor and gain for the Nth stage of a cascaded amplifier with a net excess noise factor F_{total}.[19,20] The noise contribution from the last stage, for example, is divided by the gain products in the earlier stages, in effect reducing the relative contribution of the latter stages to the overall amplifier noise. It stands to reason that the low-noise multiplication afforded by a staircase multiplier as the first stage of a cascaded amplifier would improve the total noise output for a device as compared to a non-cascaded conventional avalanche multiplier.

The design for such a cascaded amplifier device needs to achieve two distinct electric field regions in order to operate. SACM APDs accomplish this by utilizing a charge layer—a doped region used to stunt depletion through a narrow bandgap absorber.[21] This leads to a lower electric field in the absorber, reducing parasitic band-to-band tunneling of carriers. The same approach can be incorporated within a cascaded amplifier; a charge layer can be inserted between the low-field staircase and the high-field bulk multiplier regions.

Here, we report the *cascaded multiplier* APD, which employs a low-field staircase step followed by a conventional, high-field, avalanche bulk multiplier, separated by a charge layer. A multiplication gain of ~6 is reached at room temperature, determined in comparison with a step-free control device. The excess noise factor as a function of gain for the cascaded multiplier lies between that of a conventional bulk AlInAsSb (k ~ 0.01) APD and a pure AlInAsSb staircase device, suggesting that the noise benefits of a low-field staircase APD are realized in combination with a high-field avalanche multiplier, as described in Eq. (2).

AlInAsSb cascaded multiplier APDs were grown on n-type Te doped GaSb (001) substrates via molecular beam epitaxy (MBE) using the approach described in detail by Maddox *et al.*[10] The AlInAsSb digital alloys were grown as repeating periods of stable binary materials adding up to 10 monolayers (AlSb, InAs, etc.) at a growth rate of 0.75 monolayers per second. The substrate was held at a growth temperature of ~460–480 °C measured *in situ* by blackbody thermometry (k-Space BandiT). The substrate was also rotated at relatively high speeds of 22.5 rotations per minute to ensure layer uniformity. V/III beam equivalent pressure ratios of 7 for antimony and 6.2 for dimeric arsenic (over indium) were used, which corresponded to flux ratios of 4.2 and 1.9, respectively. Growth rates and lattice matching calibrations were grown and characterized in advance to ensure intended thicknesses and compositions. Structural quality of the crystal was confirmed with ω–2θ rocking curve scans using x-ray diffraction, and surface quality was confirmed using dark field microscopy (see the supplementary material). A cross-sectional schematic of the device layer structure can be seen in Fig. 1(a). The staircase region followed by the charge layer and avalanche multiplier region is shown in the energy-band vs position diagram shown in Fig. 1(b). Figure 1(c) shows the effect of the moderately doped p-type charge layer, which suppresses the electric field before and after the staircase step gradings. Devices were fabricated using standard photolithography techniques, citric acid wet etching circular mesas to 150-μm diameters, Ti/Au contact deposition, and SU-8 surface passivation.

The device structure consists of a 10^{18} cm^{-3} p-type GaSb/AlInAsSb top contact, a 500 nm undoped (UID) AlInAsSb absorber (thick enough to absorb 99% of 543 nm light), a 128 nm UID staircase step grading, a 200 nm AlInAsSb ~10^{17} cm^{-3} p-type charge layer, a 500 nm UID AlInAsSb bulk multiplier region, and a 200 nm 10^{18} cm^{-3} n-type AlInAsSb bottom contact layer. All AlInAsSb layers contain 70% Al and ~33% As except for the staircase step region (featuring compositional grading between 70% Al and 7% Al). The approximate bandgap energy of $Al_{0.7}InAsSb$ is 1.2 eV, and $Al_{0.07}InAsSb$ is 0.3 eV. A step-free control sample was grown that

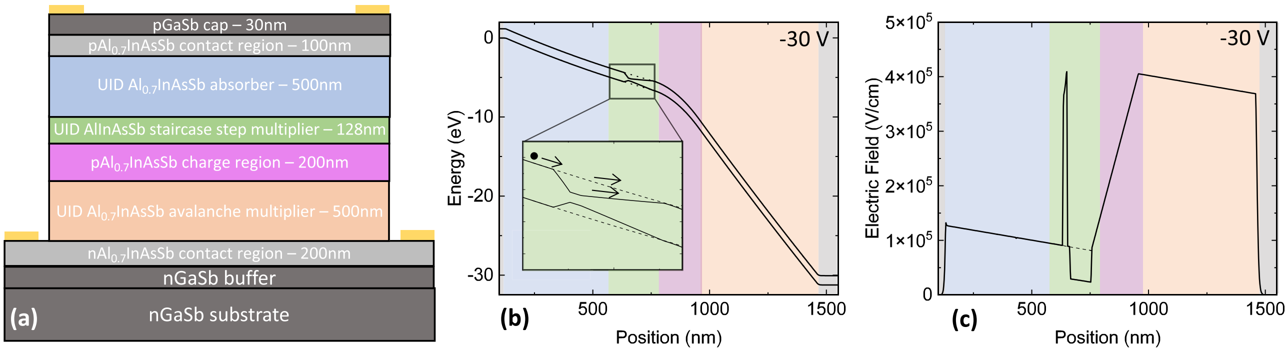

FIG. 1. (a) Schematic cross section of the 150-μm diameter mesa AlInAsSb cascaded multiplier device. (b) The energy-band diagram plotted vs position under 30 V reverse bias, lined up with the relevant layers in the cross section. The inset is the staircase step grading with electron impact ionization illustrated. (c) The conduction band electric field plotted vs position. The dashed lines in the band and electric field diagrams represent the control structure. The absorber region (blue) and the low-field staircase region (green) require a distinct electric field to the conventional bulk multiplier region (orange). The staircase region sees a large change in the electric field due to the rapid bandgap transitions corresponding with compositional gradings.

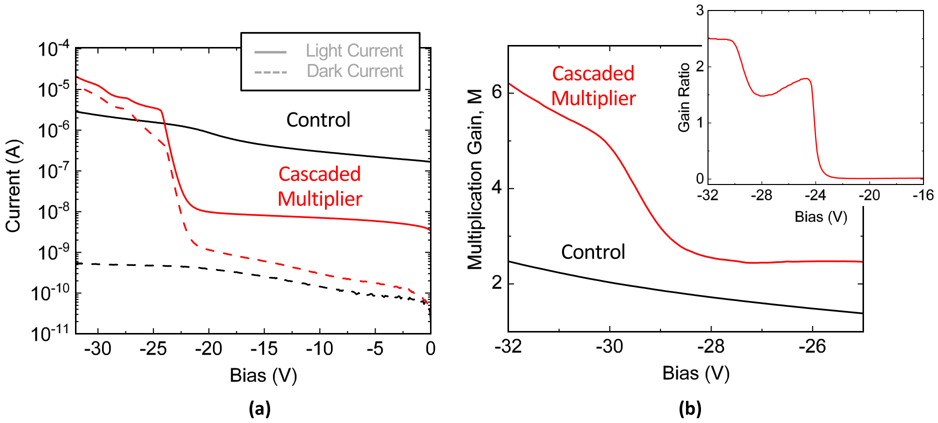

FIG. 2. (a) Current–voltage characteristics of the 150-μm mesa diameter cascade device and its control, represented by the red curves and the black curves, respectively. The solid lines indicate the total light current under 543-nm laser illumination, including the dark current contribution, and the dashed lines are the dark current characteristics. These measurements were performed under DC bias with a laser power of 31 μW. No lock-in amplifier was employed. (b) The gain curves for the cascade device and the control are again represented by the red curve and the black curve, respectively, where the gain was calculated as the photocurrent (total illuminated current minus dark current) normalized to the unity photocurrent. The inset is the gain ratio between the cascade device and the control, which corresponds to the ~2× gain contribution of the single staircase step.

suppresses staircase amplification by removing the compositional gradings present in the cascaded multiplier device, maintaining 70% Al composition for all layers. They contain identical layer thicknesses and doping values, so that the only variable is the compositional grading present in the cascaded multiplier device. The band and field diagrams of the control are shown as the dashed lines in Figs. 1(b) and 1(c). The charge layer doping was chosen to maintain a sufficiently low electric field to mitigate band-to-band tunneling in the staircase region while promoting high-field impact ionization in the bulk multiplier over a relatively wide bias range.

Device performance was characterized using room temperature current–voltage measurements performed under dark and 543-nm illumination conditions for both the cascaded multiplier and its step-free control, shown in Fig. 2(a). The punch-through depletion bias of the control device occurs at approximately -25 V, corroborated by capacitance–voltage measurements (shown in Fig. 3). The cascaded multiplier shows limited photocurrent for low reverse biases under -25 V due to charge trapping in the staircase step region. At slightly higher reverse bias these trapped charges release, and multiplication gain is observed. The cascaded multiplier dark current trend is consistent with previously demonstrated staircase devices and is attributed to the increase in band-to-band tunneling that occurs in the narrow bandgap staircase region.[16,17] However, a dark current density of ~70 mA/cm^2 at the operation bias of -31.8 V is significantly reduced from two- and three-step staircase devices, which feature room temperature dark current densities of ~170 and ~400 mA/cm^2, respectively.[17] This is attributed to the reduction in a narrow bandgap material present in step regions. The one-step staircase device with a gain of 2 exhibits a dark current density of ~21 mA/cm^2.[16] Given the similarities in the dark current trend to the pure staircase devices, this breakdown behavior suggests that the operation of the cascade device is limited by tunneling in the staircase region around -32 V.

Figure 2(b) shows the multiplication gain of the two devices. The cascaded multiplier reached a gain of ~6 prior to breakdown beyond -32 V, where the dark current contribution dominates the measured photocurrent. This is compared to a gain of ~3 by the control. The inset is a plot of the photocurrent ratio between the cascaded multiplier and the control, indicating the staircase gain contribution is the expected ~2^N ($N = 1$), consistent with previously demonstrated staircase devices.[16,17] It is worth noting the non-trivial nature of determining gain and noise in these devices; impact ionization occurs in the conventional multiplier at low bias *prior* to reaching punch-through. Thus, the unity photocurrent cannot be measured directly. To determine the unity photocurrent, the gain at punch-through was calculated in the control based on the well-known impact ionization coefficients of the material and the electric field at that bias.[22] The electric field at punch-through was determined with electro-static

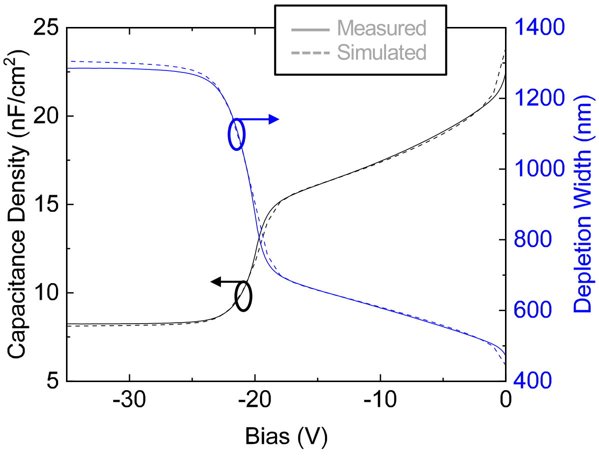

FIG. 3. Capacitance–voltage characteristics of the cascaded multiplier control device, with the calculated depletion width plotted along the right axis. These measurements were taken from a 150-μm diameter device with an HP 3275 LCR meter at 1 MHz under blackout conditions. Also shown are electrostatic simulation curves corroborating the measured data.

simulations supported by capacitance–voltage (CV) measurements, where the simulated (Lumerical CHARGE) CV profile is nearly identical to the device measurement. Using the impact ionization coefficients and the electric field calculations, the gain in the control device at punch-through was determined to be ∼1.4 at -25 V. The unity photocurrent is then the punch-through photocurrent divided by the punch-through gain, ∼1.1 μA. Calculating the gain in the cascaded multiplier device was the trivial next step of dividing the cascaded multiplier photocurrent by this unity photocurrent.

To obtain the excess noise factor, *F(M),* the shot noise power had to be scaled from the control. The shot noise power, *S*, of the cascade and control (in the absence of dark current) are as follows:

$$S_{cascade} = 2qI_{photo}R\Delta f M^2_{cascade} F(M)_{cascade}, \tag{3}$$

$$S_{control} = 2qI_{photo}R\Delta f M^2_{control} F(M)_{control}, \tag{4}$$

where q is the electron charge, R is the resistance, and Δf is the measurement bandwidth. The gain values, *M*, are known. The term $2qI_{photo}R\Delta f$ can be found by using the control structure, which has a known k-factor within a small range [and therefore $F(M)_{control}$]. Rearranging Eq. (3) gives us the following equation:

$$F(M)_{cascade} = \frac{S_{cascade}}{2qI_{photo}R\Delta f M^2_{cascade}}. \tag{5}$$

Using Eq. (5), the excess noise factor *F(M)* as a function of gain is shown in Fig. 5(a). The cascaded multiplier device shows noise values below the conventional AlInAsSb APD, which follows the expected $k \sim 0.01$ trend with multiplication gain. It does, however, lay above the pure staircase APD.[16,17] Figure 4 also indicates that the intermediate cascaded multiplier noise is further supported by Monte Carlo simulations, which predict a slightly lower multiplication gain but a very similar excess noise factor. For this, 10 000 simulation iterations were run for the cascaded multiplier at a bias value of -32 V. The simulation iterations represented individual electron–hole pairs generated according to the absorption properties of the material. Secondary carriers from impact ionization were also generated and tracked until

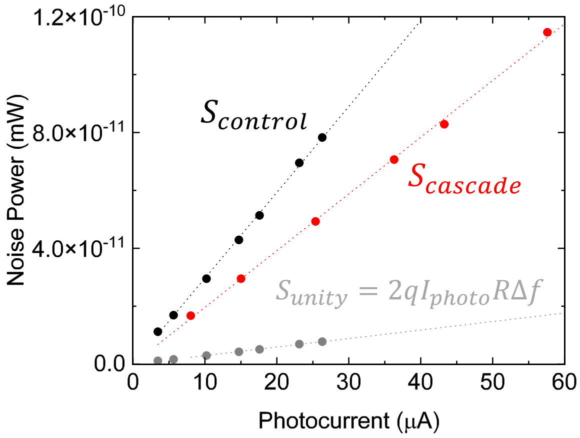

FIG. 4. Noise power measurements at fixed biases for the cascaded multiplier and control devices. The photocurrent was increased to establish a noise trend as a function of photocurrent. This was used as the term to calculate the excess noise *F(M)* for the cascaded multiplier device. These measurements were performed under 543-nm laser illumination at room temperature. The cascaded multiplier noise was amplified with a trans-impedance amplifier set to 10^5 V/A and measured with a spectrum analyzer at ∼70 kHz with a bandwidth of 47 Hz. A low frequency was used to ensure the device was not bandwidth limited.

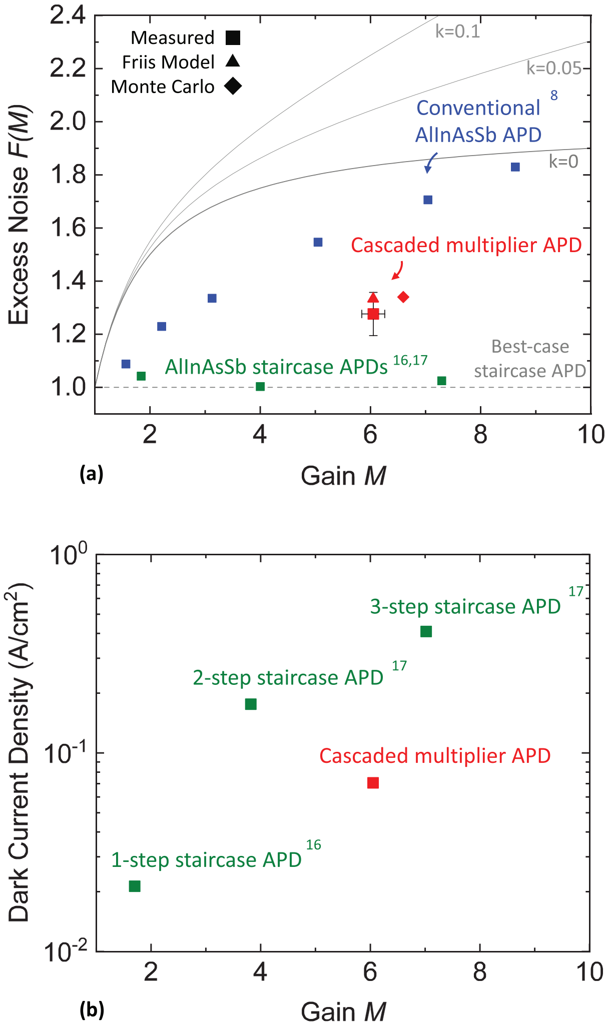

FIG. 5. (a) Excess noise factor values plotted vs the multiplication gain of various devices. The cascaded multiplier measurements (red squares) show intermediate noise between measurements of pure staircase APDs (green squares)[16,17] and a conventional AlInAsSb PIN APD (blue squares),[8] which has an impact ionization ratio of $k \sim 0.01$. The measured cascaded multiplier gain and noise values shown here are an average of seven devices from the same growth wafer and fabrication run. The error bars surrounding the cascaded multiplier gain are the extremes of those measurements, compounded by the (∼2%) uncertainty of the unity gain calculation. The vertical error bars represent the uncertainty associated with the expected $F(M)_{control}$ range, affecting the $F(M)_{cascade}$ calculation described above. This noise result is consistent with the Friis model for cascaded amplifiers (red triangle) and Monte Carlo simulations (red diamond). (b) Measured dark current comparison of AlInAsSb staircase APDs and the cascaded multiplier APD at room temperature. Plotted dark current densities are where the APDs *begin* to exhibit staircase performance (approaching 2^N gain). The dark current reduction in the cascaded multiplier APD is even greater when staircase devices are biased further to reach 2^N gain.

recombination or reaching the n-contact. Carrier transport and scattering rates were based on first-principal calculations using Fermi's Golden rule (accounting for intervalley, intravalley phonon, alloy, and impurity scattering), and impact ionization threshold energies were taken from previously reported work on AlInAsSb digital alloy P–I–N devices.[22] These values are consistent with Friis noise theory described in Eq. (2), where placing a low-noise multiplier at the early stage of a cascaded amplifier reduces the total amplification noise.

Further work should be done to increase the gain in the bulk multiplier region to higher values. This could be attempted by increasing the charge layer doping, allowing for higher bias measurements (i.e., higher field in the bulk multiplier) without suffering from staircase region breakdown. Achieving higher gain values could improve the signal-to-noise ratio in the device by leveraging the $F(M) < 2$ noise scaling afforded by the cascaded multiplier architecture. In addition, the flexible bandgap energies of AlInAsSb offer an easy path to extending the absorption wavelength of these devices to 2 μm and beyond by reducing the aluminum composition in the absorber.

The presented cascaded multiplier APD with a gain of ∼6 offers an effective way to reach improved gain above the 2^N limitation exhibited by pure staircase APDs at reduced dark current densities. Additionally, the presence of an early-stage staircase multiplier region prior to a conventional high-field bulk multiplier reduces the overall amplifier noise while supporting an increased applied electric field. As the first solid-state device of its class, the staircase cascaded multiplier APD has the potential to dramatically improve APD sensitivity moving forward.

See the supplementary material for details of post-growth characterization of the epitaxial material (including high resolution x-ray diffraction and dark field microscope images), capacitance–voltage measurements of the cascaded multiplier device, and spectral response of the cascaded multiplier device.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

J. Andrew McArthur: Conceptualization (equal); Data curation (equal); Formal analysis (lead); Investigation (lead); Methodology (equal); Validation (lead); Visualization (lead); Writing – original draft (lead); Writing – review & editing (equal). **Adam A. Dadey:** Data curation (equal); Formal analysis (equal); Investigation (supporting); Methodology (equal); Validation (supporting); Writing – review & editing (equal). **Stephen D. March:** Conceptualization (supporting); Formal analysis (supporting); Investigation (supporting); Methodology (supporting); Writing – review & editing (equal). **Andrew H. Jones:** Data curation (supporting); Formal analysis (supporting); Methodology (supporting). **Xingjun Xue:** Investigation (supporting); Methodology (supporting). **Rodolfo Salas:** Conceptualization (supporting); Formal analysis (supporting); Funding acquisition (lead); Project administration (lead); Supervision (supporting); Writing – review & editing (equal). **Joe C. Campbell:** Conceptualization (supporting); Data curation (supporting); Funding acquisition (lead); Project administration (supporting). **Seth R. Bank:** Conceptualization (equal); Funding acquisition (lead); Resources (supporting); Supervision (supporting); Visualization (supporting); Writing – original draft (supporting); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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